Apacer

RoHS Recast Compliant

Industrial microSD 6.1

CV120-MSD Product Specifications

(Kioxia TLC BiCS5 112 Layers)

October 25, 2022

Version 1.0

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Apacer

Specifications Overview:

- **Fully Compatible with SD Card Association Specifications**
  - Physical Layer Specification Ver6.1 (with CPRM)
  - Security Specification Ver4.0
- **Capacity**
  - 64, 128, 256 GB
- **Performance**[1]
  - Sequential read: Up to 90 MB/sec
  - Sequential write: Up to 85 MB/sec
  - Random read (4K): Up to 1,900 IOPS
  - Random write (4K): Up to 1,200 IOPS
- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Flash bad-block management
  - Power Failure Management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - SMART Read Refresh™
- **NAND Flash Type:** Kioxia TLC BiCS5 112 Layers
- **Backward Compatible with 3.0 and 2.0**
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Endurance (in Terabytes Written: TBW)**
  - 64 GB: 77 TBW
  - 128 GB: 149 TBW
  - 256 GB: 352 TBW
- **Temperature Range**
  - Operating:
    Standard: -25°C to 85°C
    Wide: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption**[1]
  - Operating (Max.): 110 mA
  - Standby: 165 µA
- **Bus Speed Mode:** Supports Class 10 with U3 , A2 and UHS-I[2]
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec
- **Supported Speed Class:** C10, U3 and V30
- **Physical Dimensions**
  - 15mm (L) x 11mm (W) x 1mm (H)
- **RoHS Recast Compliant**

Notes:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
2. Timing in 1.8V signaling is different from that of 3.3V signaling. Operation mode selection command is complaint with SD 3.0, referring to SDA's Part 1, Physical Layer Specification, Ver 3.01 (Section 3.9).

Table of Contents

1. General Description

Apacer microSD CV120-MSD is compatible with the microSD card version 6.1. The command list supports [Physical Layer Specification Ver6.10 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver4.0 Final] Specifications.

The microSD 6.1 card comes with 8-pin interface. It can alternate communication protocols between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption and supports capacity up to 256GB with exFAT SDXC.

Apacer microSD CV120-MSD Secure Digital 6.1 with high performance, good reliability and wide compatibility is nowadays one of the most popular cards with customized firmware techniques in semi-industrial/medical markets already.

1.1 Functional Block

The microSD contains a card controller and a memory core for the SD standard interface.

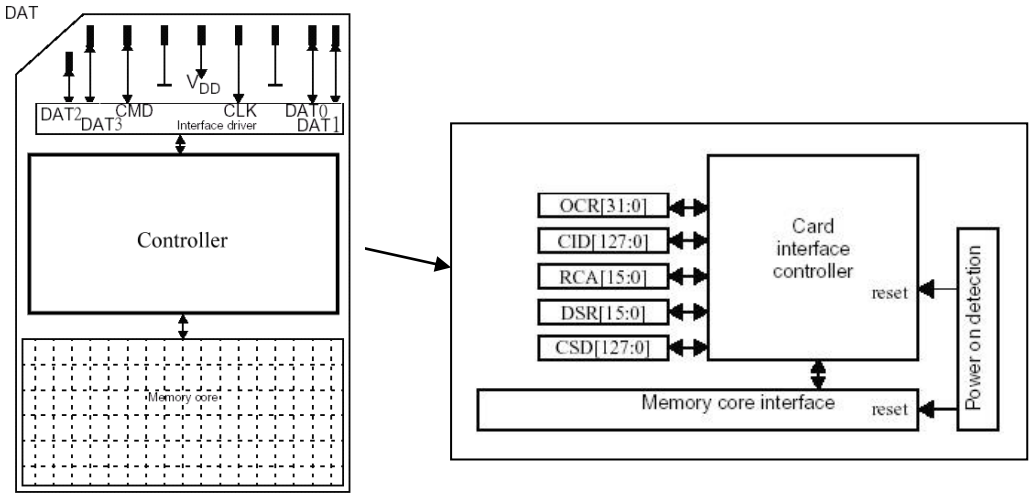


Figure 1-1 Functional Block Diagram

1.2 Flash Management

1.2.1 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. To protect data from corruption, the microSD card whose controller supports up to 100bits ECC circuits applies the advanced ECC Algorithm that can detect and correct errors occur during read process.

1.2.3 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.4. Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the microSD card, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

1.2.5 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer’s SD and microSD cards. Note that this tool can only support Apacer’s industrial SD and microSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

1.2.6 SMART Read Refresh™

Apacer’s SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

1.2.7 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve microSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

2. Product Specifications

2.1 Card Architecture

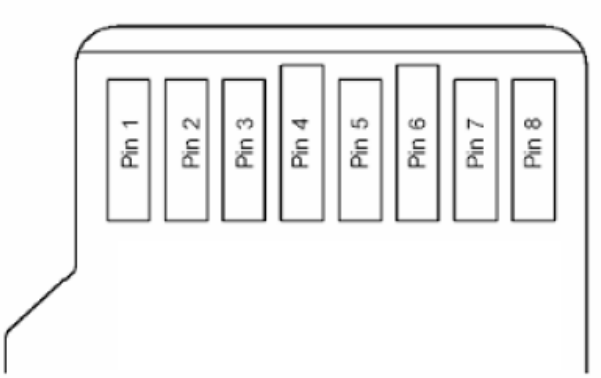


Figure 2-1 Card Architecture

2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data line[bit 2]	Reserved	
2	CD/DAT3	Card Detect/Data line [bit 3]	CS	Chip select
3	CMD	Command/Response	DI	Data in
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply voltage ground	VSS	Supply voltage ground
7	DAT0	Data line[bit 0]	DO	Data out
8	DAT1	Data line[bit 1]	Reserved	

2.3 Capacity

The following table shows the specific capacity for the microSD 6.1 card.

Table 2-2 Capacity Specifications

Capacity	Total bytes
64 GB	62,193,139,712
128 GB	124,642,131,968
256 GB	249,242,320,896

Note: Total bytes are viewed under Windows operating system and measured by SD format.

2.4 Performance

Performances of the microSD 6.1 card are shown in the table below.

Table 2-3 Performance Specifications

Capacity / Performance	64 GB	128 GB	256 GB
Sequential Read (MB/s)	90	90	90
Sequential Write (MB/s)	50	85	85
Random Read IOPS (4K)	1,900	1,900	1,900
Random Write IOPS (4K)	1,100	1,200	1,200

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.
- Performance results are measured based on USB 3.0 card reader.

2.5 Electrical

Table 2-4 Operating Voltages

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.6	V

Table 2-5 Power Consumption

Capacity / Mode	64 GB	128 GB	256 GB
Operating (mA)(Max.)	80	110	110
Standby (µA)	145	150	165

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 5.2.1.
- Power is measured based on USB 3.0 card reader.

2.6 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

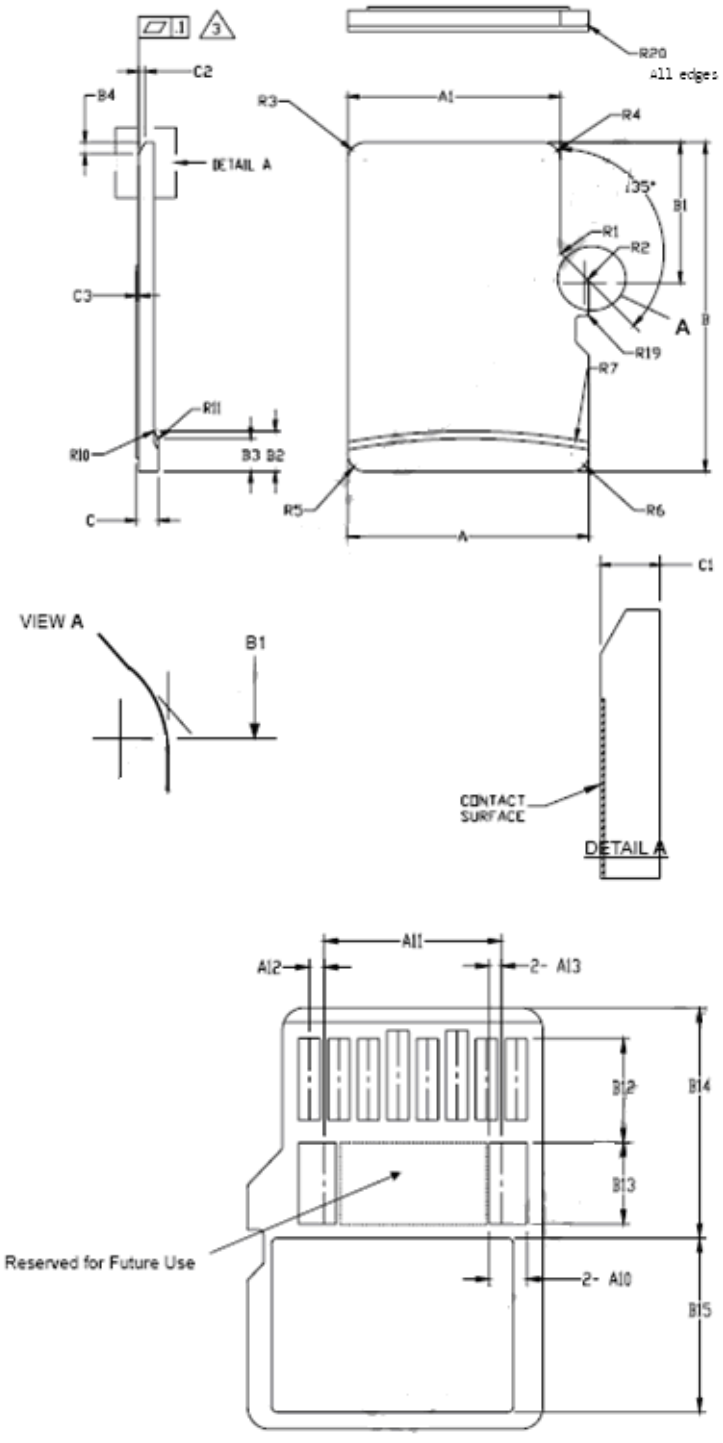
Table 2-6 Endurance Specifications

Capacity	TeraBytes Written
64 GB	77
128 GB	149
256 GB	352

Notes:
- Flash vendor guaranteed 3D TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1024 GB

3. Physical Characteristics

3.1 Physical Dimensions



	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY IS ADDITIVE TO C1 MAX. THICKNESS.

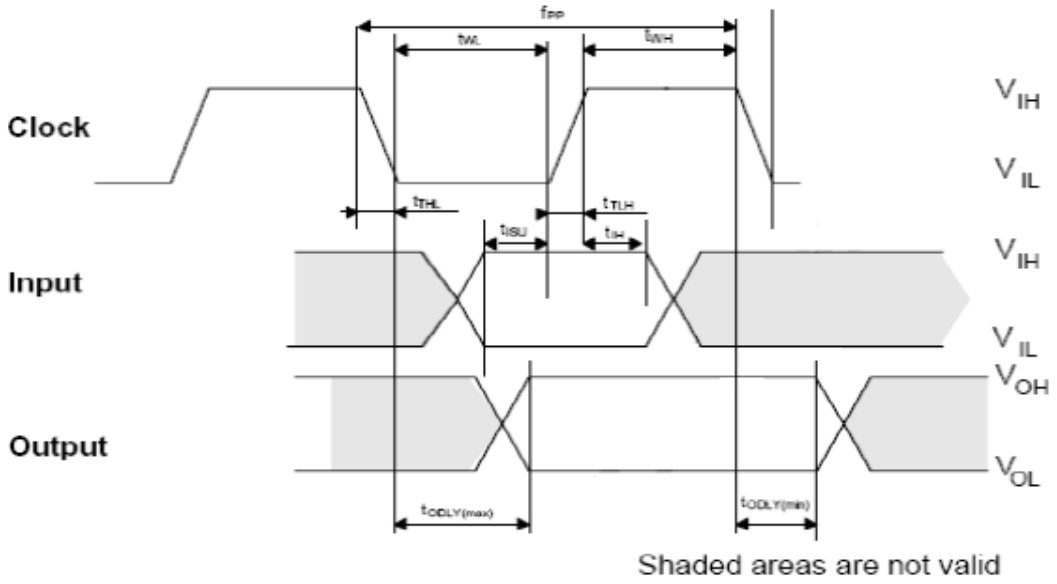
3.2 Durability Specifications

Table 3-1 Durability Specifications

Item	Specifications
Temperature	-25°C to 85°C (Standard) -40°C to 85°C (Wide)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	150cm free fall, 6 face of each
Bending	≧10N, hold 1min/5times
Torque	0.1N-m or 2.5deg, hold 5min/5times
Salt Spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Durability	10,000 times mating cycle
ESD	Pass

4. AC Characteristics

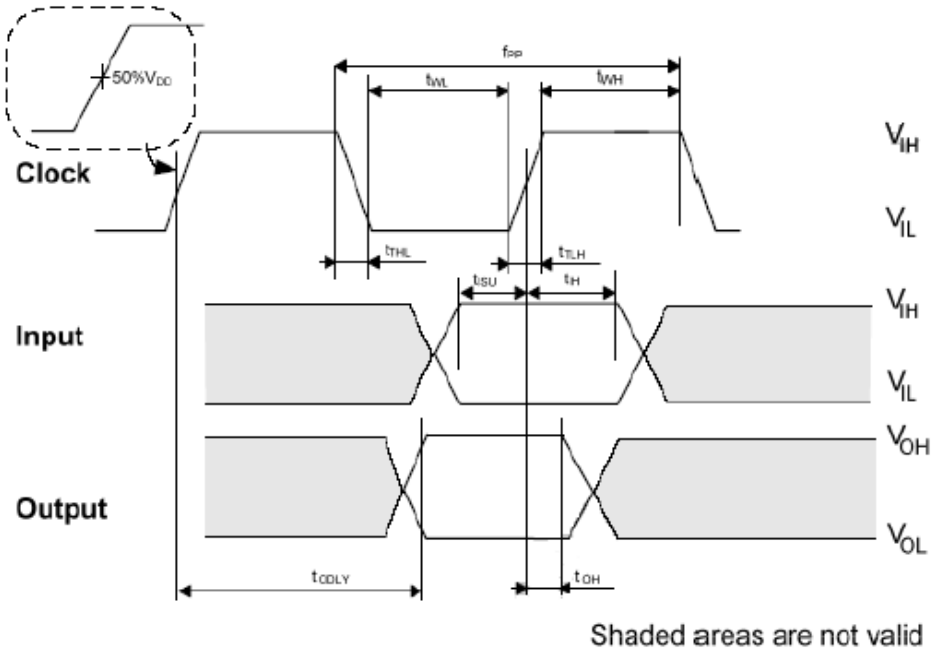
4.1 microSD Interface Timing (Default)



Symbol	Parameter	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency Data Transfer Mode	0	25	MHz	C_{card} ≤ 10 pF (1 card)
f_{OD}	Clock frequency Identification Mode	0*/100	400	kHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	10		ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	10		ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time		10	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time		10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	5		ns	C_{card} ≤ 10 pF (1 card)
t_{IH}	Input hold time	5		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode	0	14	ns	C_L ≤ 40 pF (1 card)
t_{ODLY}	Output Delay time during Identification Mode	0	50	ns	C_L ≤ 40 pF (1 card)

*0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 microSD Interface Timing (High-Speed Mode)

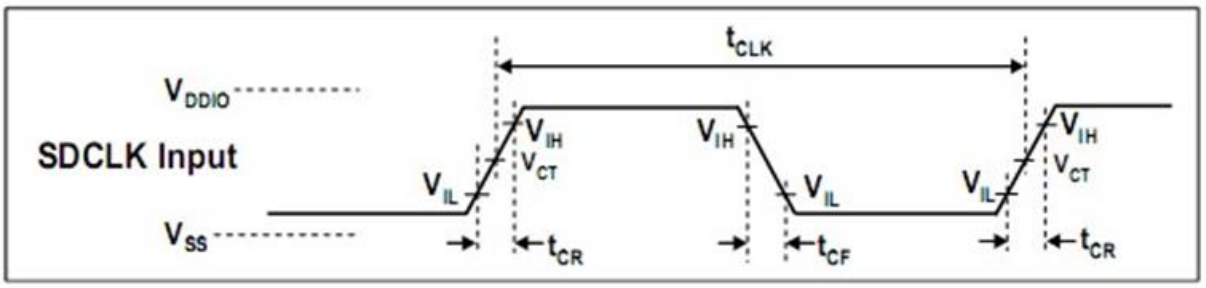


Symbol	Parameter	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency Data Transfer Mode	0	50	MHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	7		ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	7		ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time		3	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	6		ns	C_{card} ≤ 10 pF (1 card)
t_{IH}	Input hold time	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode		14	ns	C_L ≤ 40 pF (1 card)
T_{OH}	Output Hold Time	2.5		ns	C_L ≤ 15 pF (1 card)
C_L	Total System capacitance of each line*		40	pF	C_L ≤ 15 pF (1 card)

*In order to satisfy severe timing, host shall run on only one card

4.3 microSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

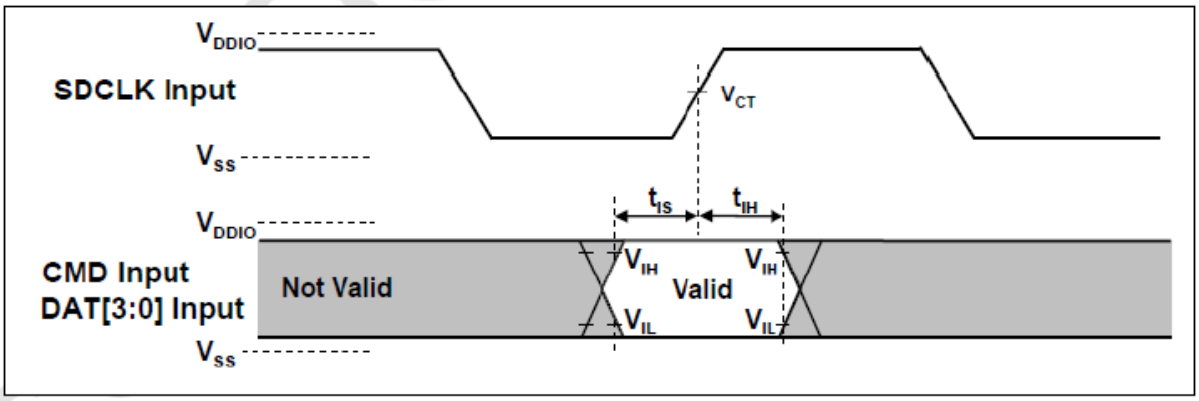
4.3.1 Input



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2 t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

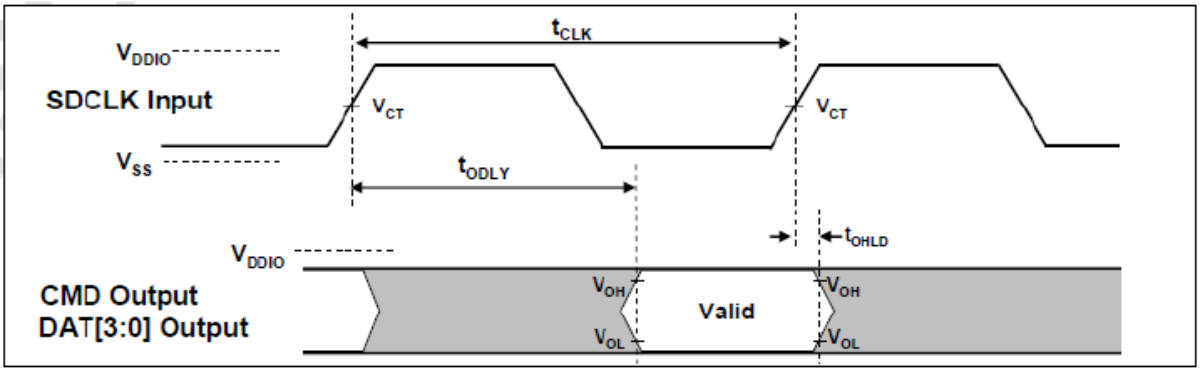
SDR50 and SDR104 Input Timing



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

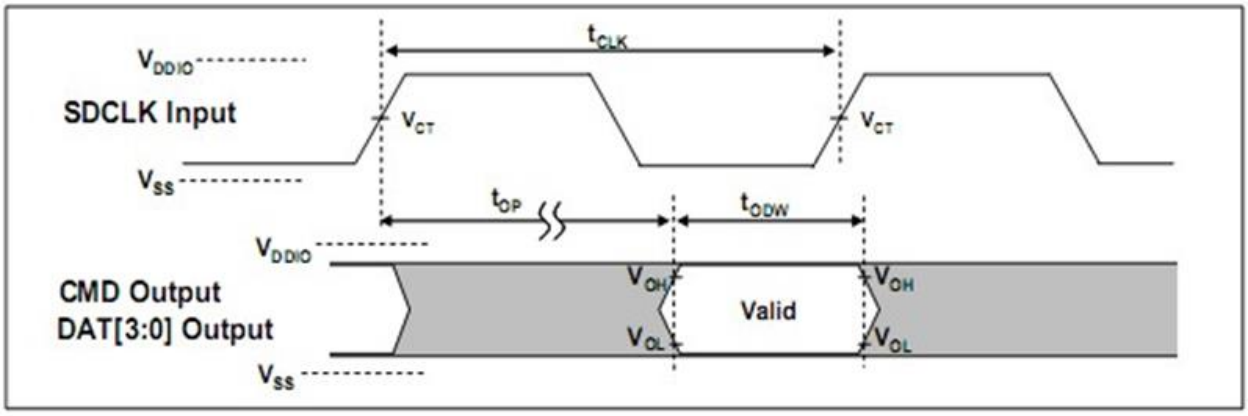
4.3.2 Output



Output Timing of Fixed Data Window

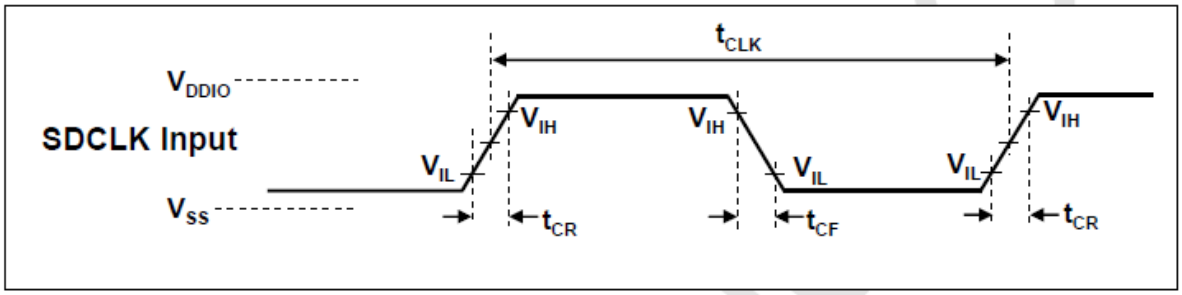
Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, C_L=30pF, using driver Type B, for SDR50.
t_{ODLY}	-	14	ns	t_{CLK} ≥20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). C_L=15pF

Output (SDR104 mode)



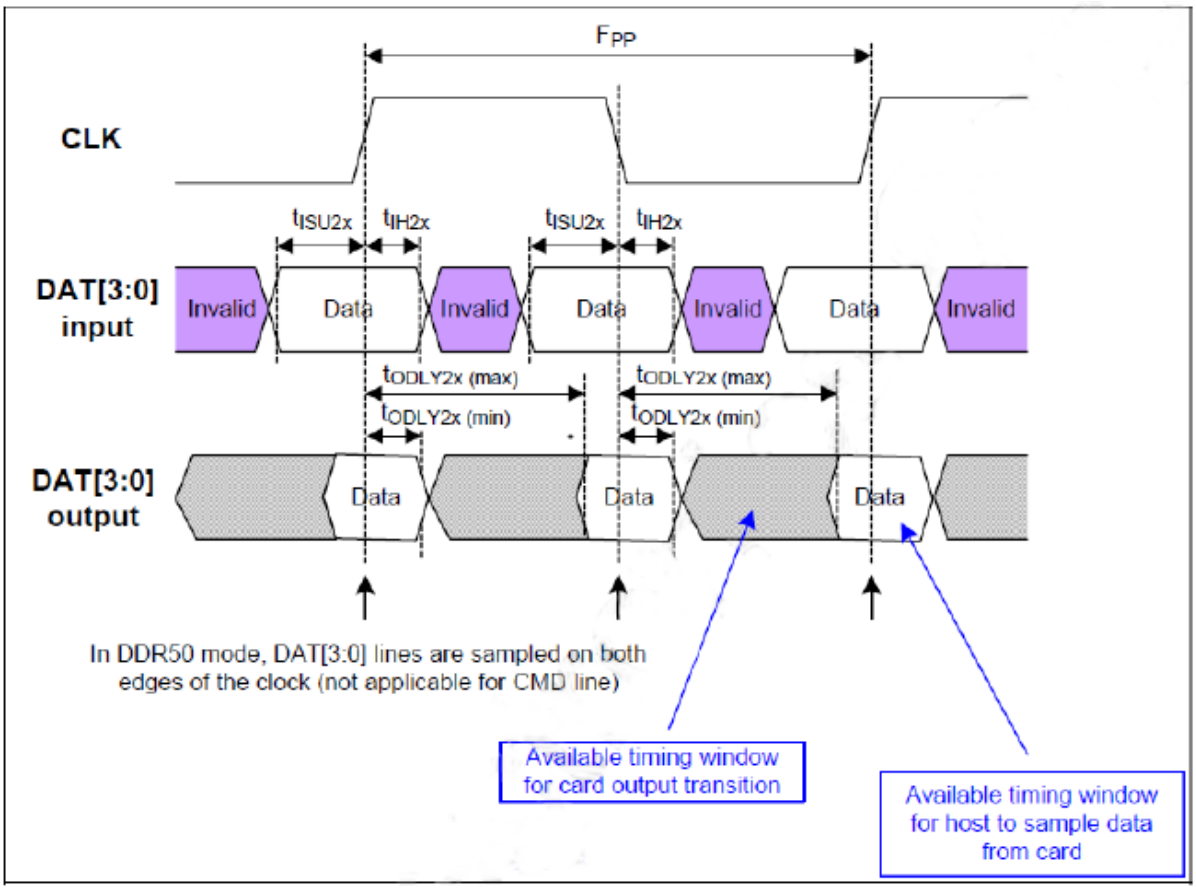
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.4 microSD Interface Timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2 t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

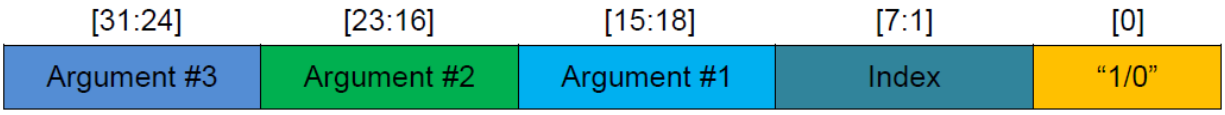
Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameter	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input setup time	3	-	ns	C_{card} ≤ 10 pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	C_{card} ≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	C_L ≤ 30 pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	C_L ≥ 15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input setup time	3	-	ns	C_{card} ≤ 10 pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	C_{card} ≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	C_L ≤ 25 pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	C_L ≥ 15 pF (1 card)

5. S.M.A.R.T.

5.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.
- Bit [7:1]: Indicates the index of the function to be executed:
  - Read Mode: Index = 0x10 Get SMART Command Information
  - Write Mode: Index = 0x08 Pre-Load SMART Command Information
- Bit [15:8]: Function argument #1 (1-byte)
- Bit [23:16]: Function argument #2 (1-byte)
- Bit [31:24]: Function argument #3 (1-byte)

5.2 Process for Retrieving SMART Data

Retrieving SMART data requires the following two commands executed in sequence and in accordance with the SD Association standard flowchart for CMD56 (see below).

Step 1: Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] “0” (Write Mode) [1:7] “0001 000” (Index = 0x08) [8:511] All ‘0’ (Reserved)	No expected data

Step 2: Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	1 sector (512 bytes) of response data byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

*Please refer to technical note for High/Low byte definition.

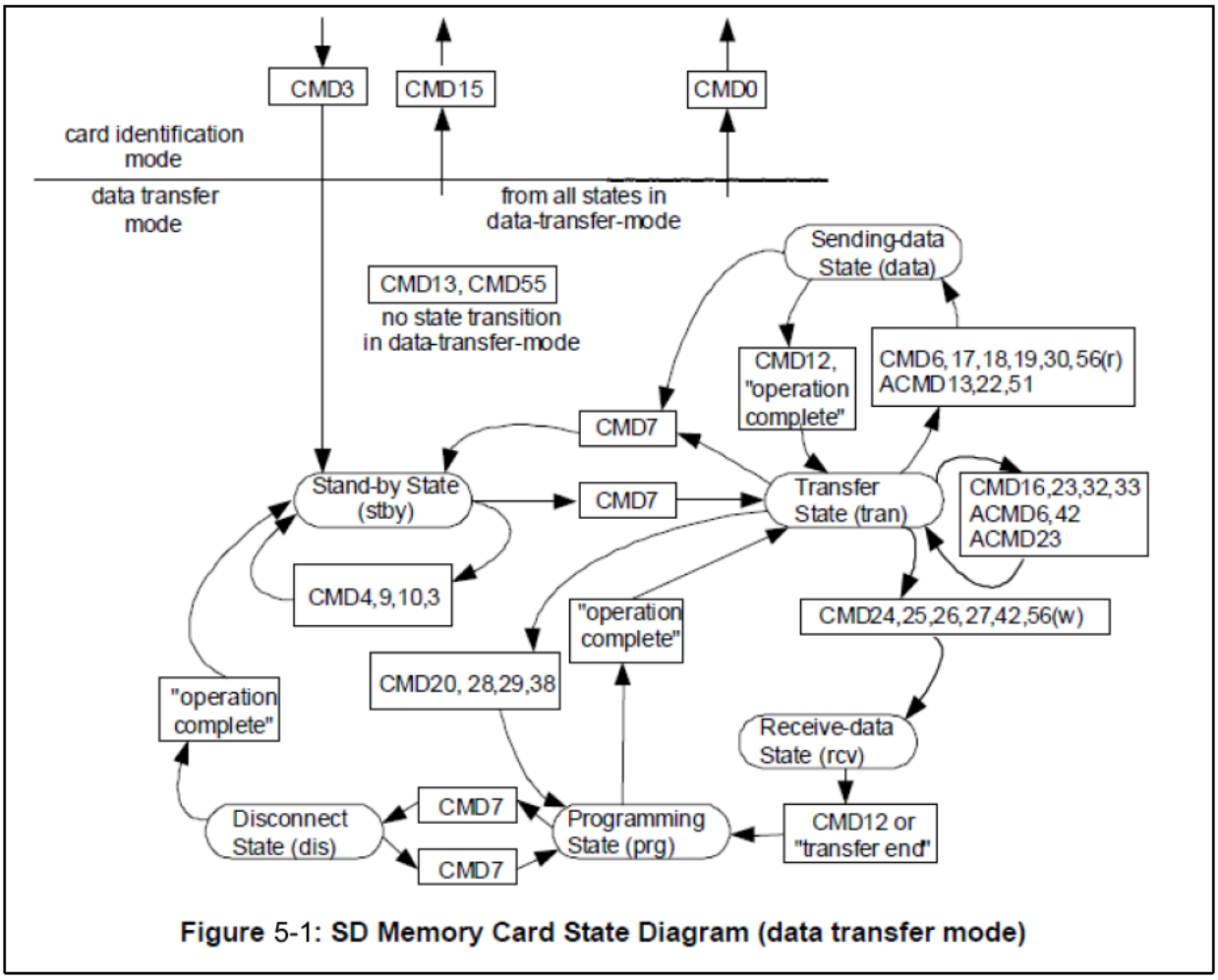


Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

6. Product Ordering Information

6.1 Product Code Designations

Apacer's CV120-MSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the CV120-MSD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	K	6	.	1	4	2	X	X	A	.	0	0	1	0	2

Code 1-3 (Product Line & Form Factor)	CV120-MSD
Code 5-6 (Model/Solution)	CV120
Code 7-8 (Product Capacity)	2G: 64GB 2H: 128GB 2J: 256GB
Code 9 (Flash Type & Product Temp)	G: 3D TLC standard temperature H: 3D TLC wide temperature
Code 10 (Product Spec)	microSD Card
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	Firmware page mode

6.2 Valid Combinations

The following table lists the available models of the CV120-MSD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Standard Temperature	Wide Temperature
64GB	AK6.142GGA.00102	AK6.142GHA.00102
128GB	AK6.142HGA.00102	AK6.142HHA.00102
256GB	AK6.142JGA.00102	AK6.142JHA.00102

Revision History

Revision	Description	Date
1.0	Initial release	10/25/2022

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