RoHS Compliant

Serial ATA Flash Drive

mSATA H1 Product Specifications

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Version 1.0

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Features:

- **Compliance with SATA Revision 3.1**
  - SATA 6.0 Gbps interface
  - Backward compatible with SATA 1.5/3.0 Gbps interfaces
  - ATA command set
- **Capacity**
  - 4, 8, 16, 32, 64 GB
- **Performance***
  - Interface burst read/write: 600 MB/sec
  - Sustained read: up to 125 MB/sec
  - Sustained write: up to 110 MB/sec
- **Flash Management**
  - Built-in hardware ECC
  - Wear leveling
  - Bad block management
  - S.M.A.R.T.
  - Power Failure Management
  - TRIM
- **NAND Flash Type:** SLC
- **MTBF:** >2,000,000 hours
- **Temperature Range**
  - Operating:
    Standard: 0°C to 70°C
    Extended: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V ± 5%
- **Power Consumption***
  - Active mode: 350 mA
  - Idle mode: 85 mA
- **Form Factor**
  - JEDEC MO-300
  - Dimensions (50.80 x 29.85 x 4.85, unit: ㎜)
- **Connector**
  - 52-pin mSATA signal connector
- **RoHS Compliant**
- **Support Device Sleep Mode (No DEVSLP Mode as optional)**

*Varies from capacities. The values addressed here are typical and may vary depending on host system settings.

Table of Contents

1. Product Description

1.1 Introduction

Apacer mSATA H1 delivers all the advantages of flash disk technology with the Serial ATA 6.0 Gbps interface and is fully compliant with the standard mSATA form factor, known as JEDEC MO-300 standard. The module is designed to operate at optimal efficiency and reliability. Its performance can reach up to 125 MB/s read and up to 110 MB/s write. Meanwhile, the power consumption of the mSATA module is much lower than traditional hard drives.

1.2 Capacity Specifications

Table 1-1 Capacity Specifications

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
4 GB	4,011,614,208	7,773	16	63	7,835,184
8 GB	8,012,390,400	15,525	16	63	15,649,200
16 GB	16,013,942,784	16,383	16	63	31,277,232
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424

*Display of total bytes varies from file systems.
**Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

1.3 Performance

Performance of mSATA H1 is shown in Table 1-2.

Table 1-2 Performance Specifications

Performance \ Capacity	4 GB	8 GB	16 GB	32 GB	64 GB
Sustained Read (MB/s)	32	60	125	120	120
Sustained Write (MB/s)	27	50	105	105	110

Note: Performance varies from flash configurations or host system settings.

1.4 Pin Assignments

Pin assignment of the mSATA H1 is shown in Figure 1-1 and described in Table 1-3.

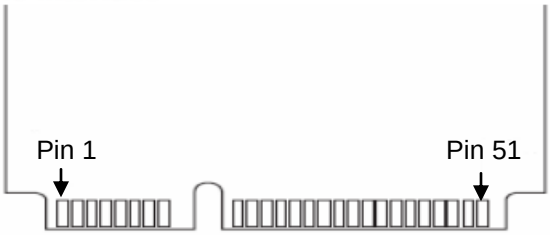
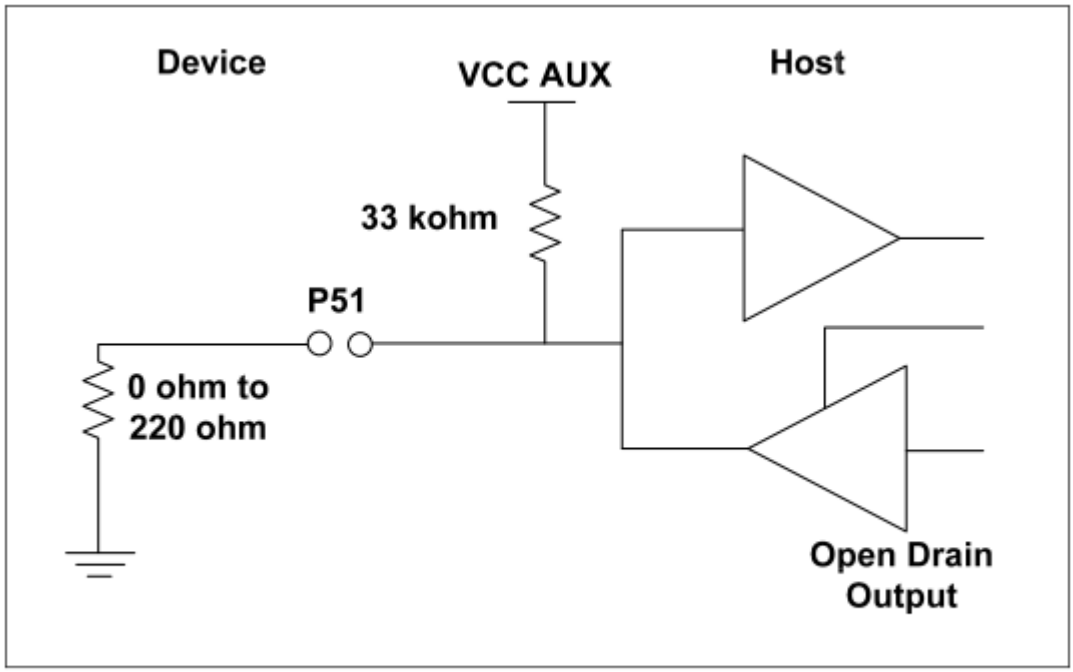


Figure 1-1 Pin Assignment

Table 1-3 Pin Assignment Description

Pin	Type	Description	Pin	Type	Description
1	Reserved	No Connect	27	GND	Ground
2	+3.3V	3.3V source	28	Reserved	No Connect
3	Reserved	No Connect	29	GND	Ground
4	GND	Ground	30	Reserved	No Connect
5	Reserved	No Connect	31	-A	Host Transmitter Differential Signal Pair
6	Reserved	No Connect	32	Reserved	No Connect
7	Reserved	No Connect	33	+A	Host Transmitter Differential Signal Pair
8	Reserved	No Connect	34	GND	Ground
9	GND	Ground	35	GND	Ground
10	Reserved	No Connect	36	Reserved	No Connect
11	Reserved	No Connect	37	GND	Ground
12	Reserved	No Connect	38	Reserved	No Connect
13	Reserved	No Connect	39	+3.3V	3.3V source
14	Reserved	No Connect	40	GND	Ground
15	GND	Ground	41	+3.3V	3.3V source
16	Reserved	No Connect	42	Reserved	No Connect
17	Reserved	No Connect	43	Device Type	No Connect
18	GND	Ground	44	DEVSLP	Device Sleep, input. If driven high the host will inform the SSD to enter a low power state.
19	Reserved	No Connect	45	Reserved	No Connect
20	Reserved	No Connect	46	Reserved	No Connect
21	GND	Ground	47	Reserved	No Connect
22	Reserved	No Connect	48	Reserved	No Connect
23	+B	Host Receiver Differential Signal Pair	49	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Ground
25	-B	Host Receiver Differential Signal Pair	51*	Detect	0 ohm
26	GND	Ground	52	+3.3V	3.3V source

*Note about Pin51: It is a presence detection pin that shall be connected to GND by a 0 ohm to 220 ohm Resistor on device. Please see the diagram below.



Bi-directional host-side implementation of P51 for compatibility with non-mSATA devices (informative)

2. Software Interface

2.1 Command Set

Table 2-1 summarizes the ATA commands supported by mSATA H1.

Table 2-1 Command Set

Code	Command	Code	Command
E5h	Check power mode	F6h	Security Disable Password
06h	Data Set management	F3h	Security Erase Prepare
B1H	DCO	F4h	Security Erase Unit
92h	Download Microcode PIO	F5h	Security Freeze Lock
93h	Download Microcode DMA	F1h	Security Set Password
90h	Execute drive diagnostic	F2h	Security Unlock
E7h	Flush cache	70h	Seek
EAh	Flush cache Ext	EFh	Set features
ECh	Identify device	F9h	Set Max Address
E3h	Idle	37h	Set Max Address Ext
E1h	Idle immediate	C6h	Set multiple mode
91h	Initialize drive parameters	E6h	Sleep
E4h	Read buffer	B0h	Smart
C9h	Read DMA (w/o retry)	E2h	Standby
C8h	Read DMA (w/retry)	E0h	Standby immediate
25h	Read DMA Ext	E8h	Write buffer
60h	Read FPDMA QUEUED	CBh	Write DMA (w/o retry)
2Fh	Read Log Ext	CAh	Write DMA (w/retry)
C4h	Read multiple	35h	Write DMA Ext
29h	Read multiple Ext	3Dh	Write DMA FUA Ext
F8h	Read native max address	61h	Write FPDMA QUEUED
27h	Read native max Ext	3Fh	Write Log Ext
21h	Read sector(s) (w/o retry)	C5h	Write multiple
20h	Read sector(s) (w/retry)	39h	Write multiple Ext
24h	Read sector(s) Ext	CEh	Write multiple FUA Ext
42h	Read Verify Ext	31h	Write sector(s) (w/o retry)
41h	Read verify sector(s) (w/o retry)	30h	Write sector(s) (w/retry)
40h	Read verify sector(s) (w/retry)	34h	Write sector(s) Ext
10h	Recalibrate	45h	Write uncorrectable

Note. Security command will only be workable when device runs in non-OPAL compliant mode.

2.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

3. Flash Management

3.1 Error Correction/Detection

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, this mSATA SSD module applies the BCH ECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption. This device can correct up to 72bit/1K data.

3.2 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

3.3 Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Apacer provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

3.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple flush cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

3.5 TRIM

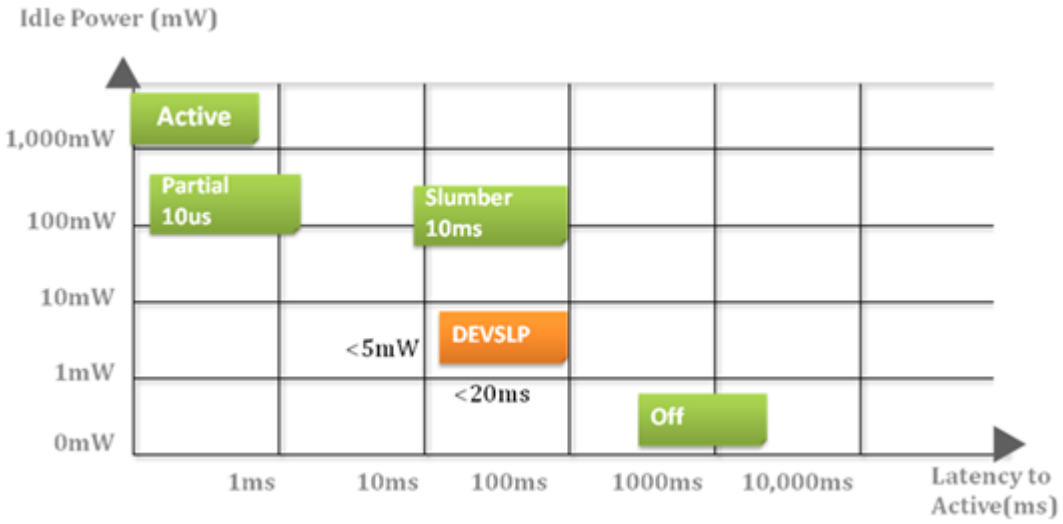
TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

3.6 Page Mapping FTL

Page mapping is a 4K-based firmware technology whose essence lies in the ability to gather data, distribute the data into 4KB blocks automatically, and then schedule the data to be evenly written. This implementation is also evidenced by JEDEC that 4KB is the most frequently used block size for data read/write access, constituting 67% of server workload. Thus, 4K page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

3.7 DEVSLP (DevSleep or DEVSLP) Mode

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating pin 44 as DEVSLP signal with an aim to reducing power consumption.



3.8 Secure Erase

Secure Erase is a standard ATA command and will write all “0xFF” to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

Note: Secure erase command belongs to ATA security command.

4. Environment Specifications

4.1 Environmental

Table 4-1 Environmental Specifications

Environment		Specifications
Temperature	Operating	Standard: 0°C to 70°C Extended: -40°C to 85°C
	Storage	-40°C to 100°C (Storage)
Shock	Operation	50G, 11ms
	Non-operation	1500G, 0.5ms
Vibration	Operation	7.69 Grms, 20~2000 Hz/random (compliant with MIL-STD-810G)
	Non-operation	4.02 Grms, 15 ~ 2000 Hz/sine (compliant with MIL-STD-810G

Note: Shock and Vibration specifications are subject to change without notice.

4.2 Mean Time Between Failures (MTBF)

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of this mSATA device is higher than 2,000,000 hours.

4.3 Certification and Compliance

mSATA H1 complies with the following standards:

- SATA Revision 3.1
- RoHS
- ATA/ATAPI
- FCC
- CE
- BSMI
- MIL-STD-810G

5. Electrical Characteristics

5.1 Operating Voltage

Table 5-1 lists the supply voltage for mSATA H1.

Table 5-1 Operating Voltage

Parameter	Conditions
Supply Voltage	3.3V ± 5%

5.2 Power Consumption

Table 5-2 lists the power consumption for mSATA H1.

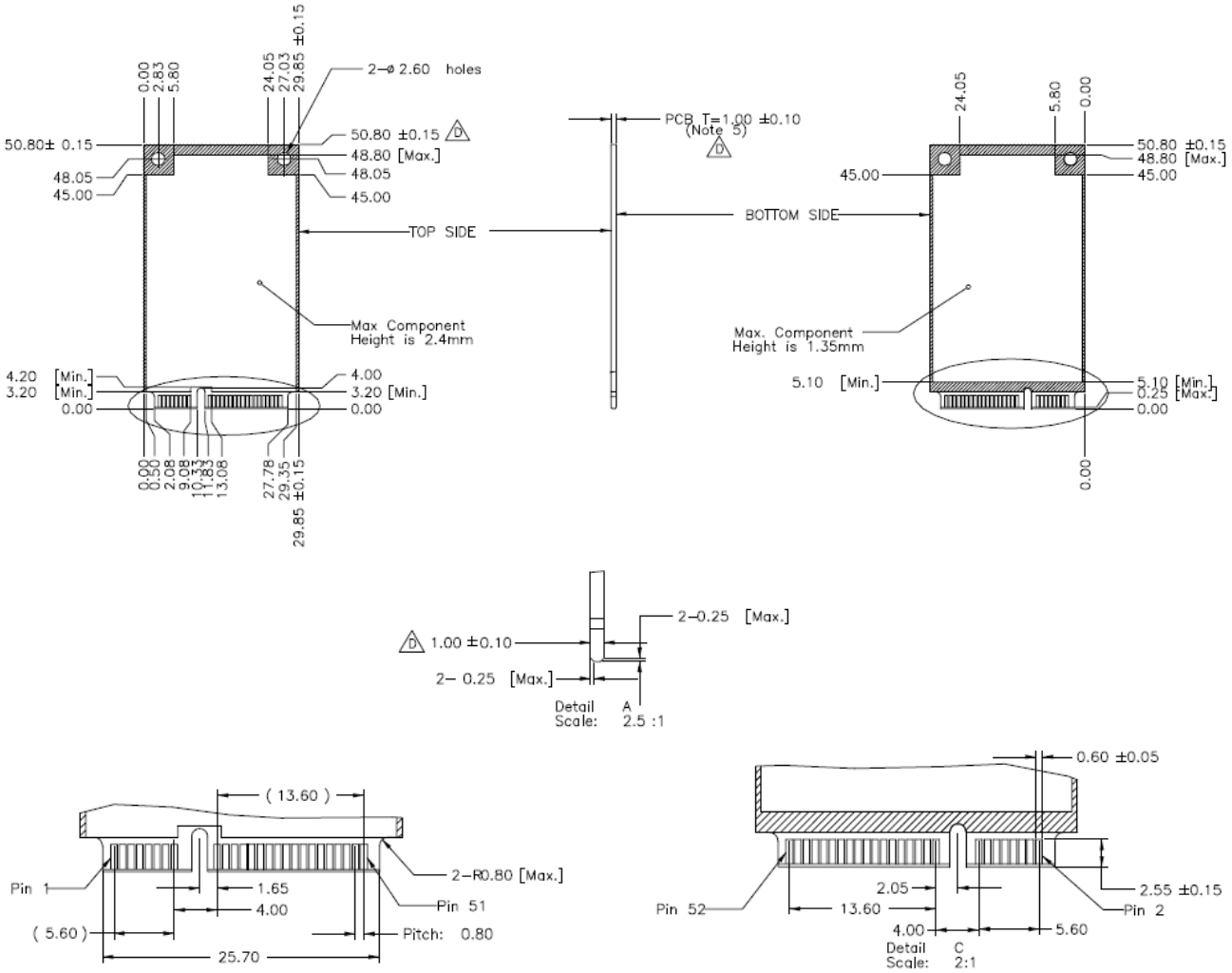
Table 5-2 Power Consumption (typical)

Mode \ Capacity	4 GB	8 GB	16 GB	32 GB	64 GB
Active (mA)	195	230	315	330	350
Idle (mA)	85	85	85	85	85

Note: Power consumptions may vary depending on host system settings.

6. Mechanical Specifications

6.1 Dimensions



Unit: mm
Tolerance: ± 0.2

7. Product Ordering Information

7.1 Product Code Designation

AP M xxxG M 1 A N - XX T X

- **Operating Temperature Range**
  Blank: Standard Temperature
  W: Extended Temperature
- **Flash Type**
- **Version Control**
- **N: Standard**
- **A: Standard**
- **Solution Version**
- **Form Factor**
  M: mSATA H1
- **Capacity**
  004G = 4 GB
  008G = 8 GB
  016G = 16GB
  032G = 32GB
  064G = 64GB
- **mSATA**
- **Apacer Product Code**

7.2 Valid Combinations

7.2.1 With DEVSLP (Standard)

Capacity	Standard Temperature	Extended Temperature
4GB	APM004GM1AN-W2T	APM004GM1AN-W2TW
8GB	APM008GM1AN-W2T	APM008GM1AN-W2TW
16GB	APM016GM1AN-W2T	APM016GM1AN-W2TW
32GB	APM032GM1AN-W2T	APM032GM1AN-W2TW
64GB	APM064GM1AN-W2T	APM064GM1AN-W2TW

7.2.2 Without DEVSLP (Optional)

Capacity	Standard Temperature	Extended Temperature
4GB	APM004GM1AN-W1T	APM004GM1AN-W1TW
8GB	APM008GM1AN-W1T	APM008GM1AN-W1TW
16GB	APM016GM1AN-W1T	APM016GM1AN-W1TW
32GB	APM032GM1AN-W1T	APM032GM1AN-W1TW
64GB	APM064GM1AN-W1T	APM064GM1AN-W1TW

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	9/1/2016

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