

***RoHS Compliant***

## **Serial ATA Flash Drive**

***SM220-300B mSATA Mini Product Specifications (Toshiba 15nm)***

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**Version 1.3**



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## Features:

- **Serial ATA Compliance**
  - Serial ATA Revision 3.1
  - SATA 6.0 Gbps interface
  - Backward compatible with SATA 1.5/3.0 Gbps interfaces
  - ATA-8 command set
- **Capacity**
  - 8, 16, 32, 64, 128 GB
- **Performance\***
  - Burst read/write: 600 MB/sec
  - Sustained read: Up to 280 MB/sec
  - Sustained write: Up to 180 MB/sec
  - Random read (4K): up to 47,000 IOPS
  - Random write (4K): up to 45,000 IOPS
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Flash bad-block management
  - Page Mapping FTL
  - S.M.A.R.T.
  - Power Failure Management
  - ATA Secure Erase
  - TRIM
- **NAND Flash Type:** MLC
- **MTBF:** > 1,000,000 hours
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Extended: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3V  $\pm$  5%
- **Power Consumption\***
  - Active: 490 mA
  - Idle: 110 mA
- **Form Factor**
  - mSATA mini, JEDEC MO-300B
  - Dimensions (29.85 x 26.80 x 3.95, unit: mm)
- **Connector**
  - 52-pin mSATA connector
- **Shock & Vibration\*\***
  - Shock: 1,500G
  - Vibration: 15G
- **DRAM Cache for Enhanced Random Performance**
- **SATA Power Management Modes**
- **LED Indicators for Drive Behavior**
- **Thermal Sensor (optional)**
- **RoHS Compliant**

\*Varies from capacities. The values addressed here are typical and may vary depending on settings and platforms.

\*\*Non-operating

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# 1. Product Description

## 1.1 Introduction

Apacer SM220-300B is a well-balanced solid-state disk (SSD) drive with compact form factor (JEDEC MO-300B) and great performance. Designed in SATA 6.0 Gbps interface, the mSATA SSD is able to deliver exceptional read/write speed, making it the ideal companion for heavy-loading embedded or server operations with space constraints for host computing systems. For data efficiency, the internal controlling unit of the mSATA SSD is engineered with DRAM for enhanced random performance. In regard of reliability, the drive comes with various implementations including powerful hardware ECC engine, power saving modes, wear leveling, flash block management, S.M.A.R.T., TRIM, and power failure management.

## 1.2 Functional Block Diagram

SM220-300B drive includes a single-chip SATA Controller and the flash media, as well as the SATA standard interface. The controller integrates the flash management unit with the controller itself to support multi-channel, multi-bank flash arrays. Figure 1-1 shows the functional block diagram.

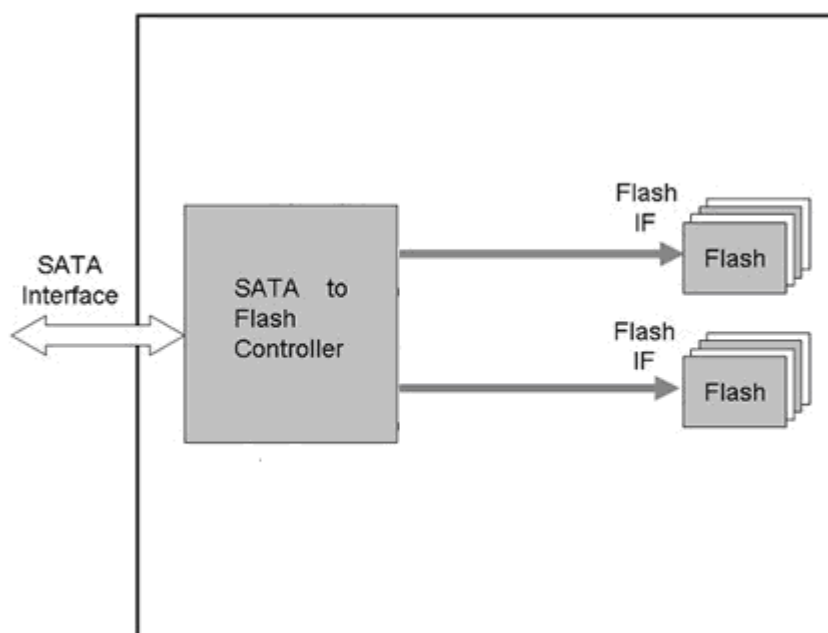


Figure 1-1 Functional Block Diagram

## 1.3 Capacity Specifications

Capacity specifications of SM220-300B product family are available as shown in Table 1-1. It lists the specific capacity, the default numbers of logical cylinders and heads, and the number of logical sectors per track for each product line.

**Table 1-1 Capacity Specifications**

Capacity	Total Bytes*	Cylinders	Heads	Sectors	Max LBA*
8 GB	8,012,390,400	15,525	16	63	15,649,200
16 GB	16,013,942,784	16,383	16	63	31,277,232
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424
128 GB	128,035,676,160	16,383	16	63	250,069,680

\*Display of total bytes varies from file systems.

\*\*Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.

\*\*Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

## 1.4 Performance Specifications

Performance of SM220-300B is shown in Table 1-2.

**Table 1-2 Performance Specifications**

Capacity Performance	8 GB	16 GB	32 GB	64 GB	128 GB
<b>Sustained Read (MB/s)</b>	115	220	220	280	260
<b>Sustained Write (MB/s)</b>	26	50	45	90	180
<b>Random Read IOPS (4K)</b>	15,000	26,000	25,000	46,000	47,000
<b>Random Write IOPS (4K)</b>	4,000	10,000	11,000	22,000	45,000

Note: Performance varies from flash configurations and/or platform settings.

## 1.5 Pin Assignments

Pin assignment of the SM220-300B is shown in Figure 1-2 and described in Table 1-3.

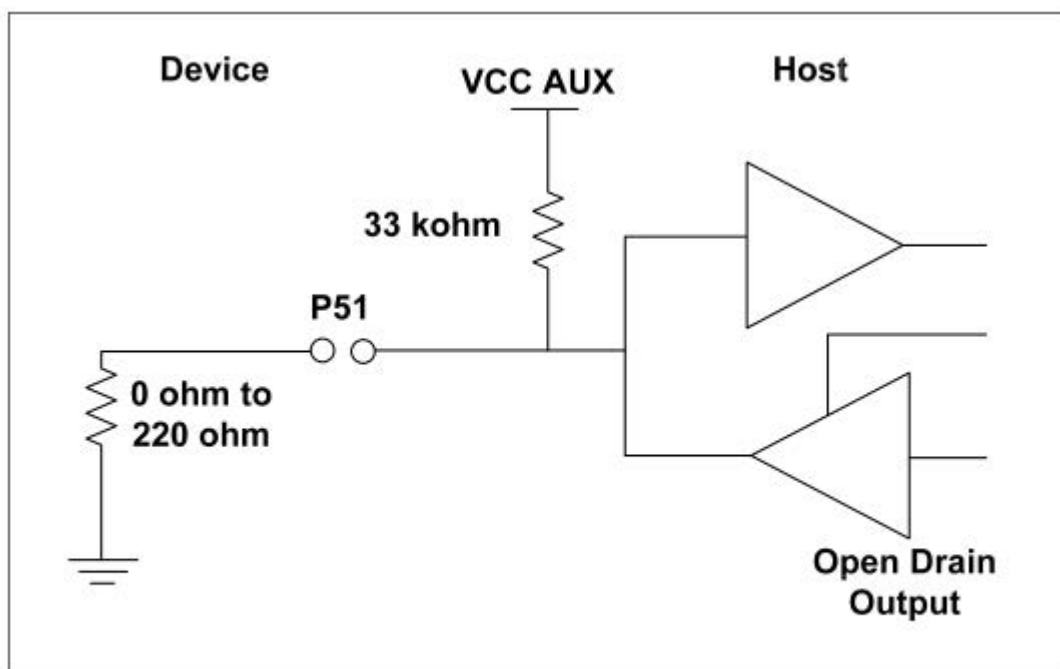


**Figure 1-2** Pin Assignment

**Table 1-3** Pin Assignment Description

Pin	Type	Description	Pin	Type	Description
1	Reserved	No Connect	27	GND	Ground
2	+3.3V	3.3V source	28	Reserved	No Connect
3	Reserved	No Connect	29	GND	Ground
4	GND	Ground	30	Reserved	No Connect
5	Reserved	No Connect	31	-A	Host Transmitter Differential Signal Pair
6	Reserved	No Connect	32	Reserved	No Connect
7	Reserved	No Connect	33	+A	Host Transmitter Differential Signal Pair
8	Reserved	No Connect	34	GND	Ground
9	GND	Ground	35	GND	Ground
10	Reserved	No Connect	36	Reserved	No Connect
11	Reserved	No Connect	37	GND	Ground
12	Reserved	No Connect	38	Reserved	No Connect
13	Reserved	No Connect	39	+3.3V	3.3V source
14	Reserved	No Connect	40	GND	Ground
15	GND	Ground	41	+3.3V	3.3V source
16	Reserved	No Connect	42	Reserved	No Connect
17	Reserved	No Connect	43	Device Type	No Connect
18	GND	Ground	44	Reserved	No Connect
19	Reserved	No Connect	45	Reserved	No Connect
20	Reserved	No Connect	46	Reserved	No Connect
21	GND	Ground	47	Reserved	No Connect
22	Reserved	No Connect	48	Reserved	No Connect
23	+B	Host Receiver Differential Signal Pair	49	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Ground
25	-B	Host Receiver Differential Signal Pair	51*	Detect	0 ohm
26	GND	Ground	52	+3.3V	3.3V source

\*Notes about Pin51: It is a presence detection pin that shall be connected to GND by a 0 ohm to 220 ohm Resistor on device. Please see the diagram below.



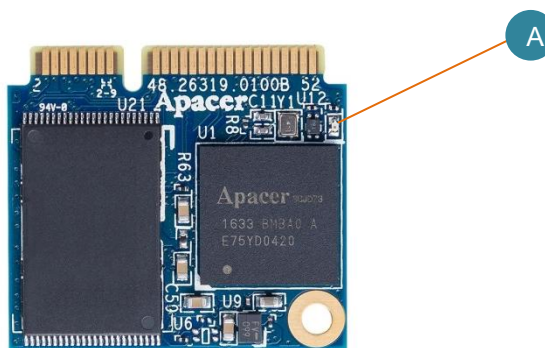
BI-directional host-side implementation of P51 for compatibility with non-mSATA devices (Informative)

## 1.6 LED Indicator Behavior

The behavior of the SM220-300B LED indicators is described in Table 1-4.

Table 1-4 LED Behavior

Location	Status	Description
LED A	Blinking	LED blinking when SSD read/write access





## 2. Software Interface

### 2.1 Command Set

Table 2-1 summarizes the ATA commands supported by SM220-300B.

**Table 2-1** Command Set

Code	Command	Code	Command
E5h	Check Power Mode	F4h	Security Erase Unit
90h	Execute Diagnostics	F5h	Security Freeze Lock
E7h	Flush Cache	F1h	Security Set Password
ECh	Identify Device	F2h	Security Unlock
E3h	Idle	7Xh	Seek
E1h	Idle Immediate	EFh	Set Features
91h	Initialize Device Parameters	C6h	Set Multiple Mode
C8h	Read DMA	E6h	Sleep
25h	Read DMA EXT	B0h	SMART
60h	Read FPDMA Queued	E2h	Standby
47h	Read Log DMA EXT	E0h	Standby Immediate
2Fh	Read Log EXT	CAh	Write DMA
C4h	Read Multiple	35h	Write DMA EXT
20h or 21h	Read Sectors	61h	Write FPDMA Queued
40h or 41h	Read Verify Sectors	57h	Write Log DMA EXT
10h	Recalibrate	3Fh	Write Log EXT
F6h	Security Disable Password	C5h	Write Multiple
F3h	Security Erase Prepare	30h or 31h	Write Sectors

### 2.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

## Serial ATA Flash Drive APMxxxGNEAN-3GTM1XX



Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	Enable/Disable Attribute Autosave
D4h	Execute Off-line Immediate
D5h	Read Log (optional)
D6h	Write Log (optional)
D8h	Enable Operations
D9h	Disable operations
DAh	Return Status

### General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status flag
3	Value
4	Worst
5*-11	Raw Data

\*Byte 5: LSB

### SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on hours
12 (0x0C)	Power cycle count
163 (0xA3)	Max. erase count
164 (0xA4)	Avg. erase count
166 (0xA6)	Total later bad block count
167 (0xA7)	SSD Protect Mode (vendor specific)
168 (0xA8)	SATA PHY Error Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
241 (0xF1)	Total sectors of write

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## 3. Flash Management

### 3.1 Error Correction/Detection

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SM220-300B implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 40 bits error in 1K bytes.

### 3.2 Bad Block Management

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Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

### 3.3 Global Wear Leveling

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Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

### 3.4 Power Failure Management

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Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

### 3.5 ATA Secure Erase

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ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

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## 3.6 TRIM

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TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

## 3.7 Page Mapping FTL

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Page mapping is a 4K-based firmware technology whose essence lies in the ability to gather data, distribute the data into 4KB blocks automatically, and then schedule the data to be evenly written. This implementation is also evidenced by JEDEC that 4KB is the most frequently used block size for data read/write access, constituting 67% of server workload. Thus, 4K page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

## 3.8 SATA Power Management

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By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10  $\mu$ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management

Note: The behaviors of power management features would depend on host/device settings.

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## 4. Environmental Specifications

### 4.1 Environments

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SM220-300B environmental specifications follow the US Military Standard MIL-STD-810F, as shown in table below.

**Table 4-1** Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Standard); -40°C to 85°C (Extended)
	-40°C to 100°C (Non-operating)
Vibration	Non-operating: sine wave, 15(G), 10~2000(Hz), Operating: Random , 7.69(Grms), 20~2000(Hz)
Shock	Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms

### 4.2 Mean Time Between Failures (MTBF)

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Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in mSATA. The prediction result for the SM220-300B is more than 1,000,000 hours.

Note: The prediction is based on Bellcore analysis method by assuming device failure rate can be generated by the sum of failure rates in each component.

### 4.3 Certification and Compliance

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SM220-300B complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810F

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## 5. Electrical Characteristics

### 5.1 Operating Voltage

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Table 5-1 lists the supply voltage for SM220-300B.

**Table 5-1** Operating Voltage

Parameter	Conditions
Supply Voltage	3.3V $\pm$ 5% (3.135 - 3.465V)

### 5.2 Power Consumption

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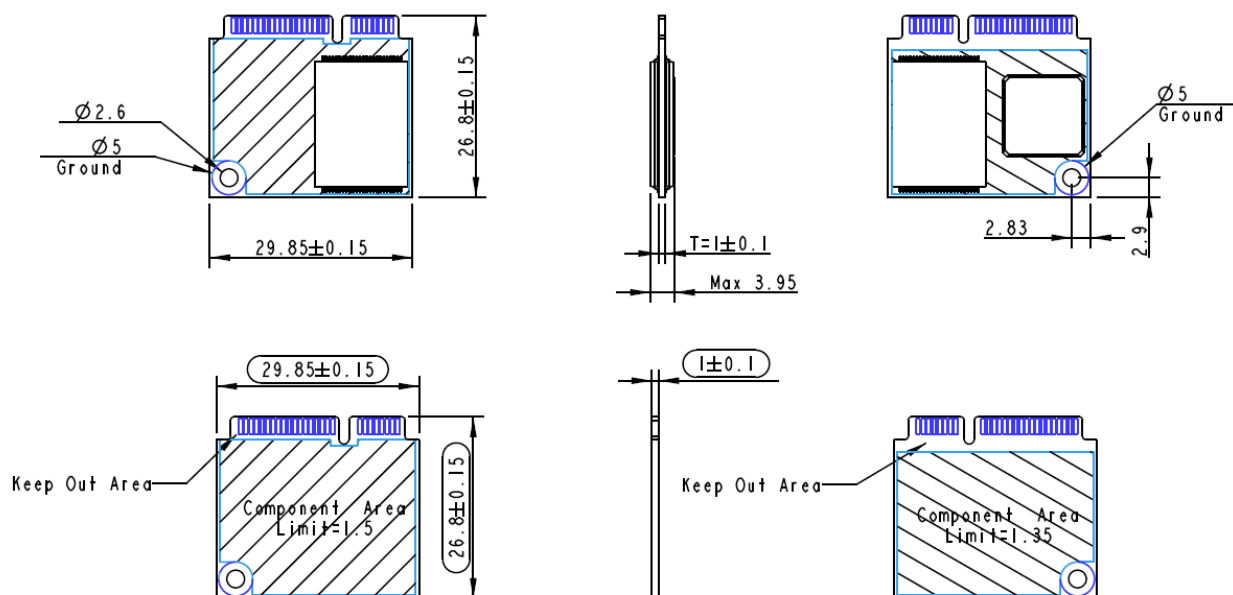
**Table 5-2** Power Consumption (typical)

Mode \ Capacity	8 GB	16 GB	32 GB	64 GB	128 GB
Active (mA)	175	265	325	485	490
Standby (mA)	80	100	100	100	110

Note: Power consumption may vary from flash configurations and/or platform settings.

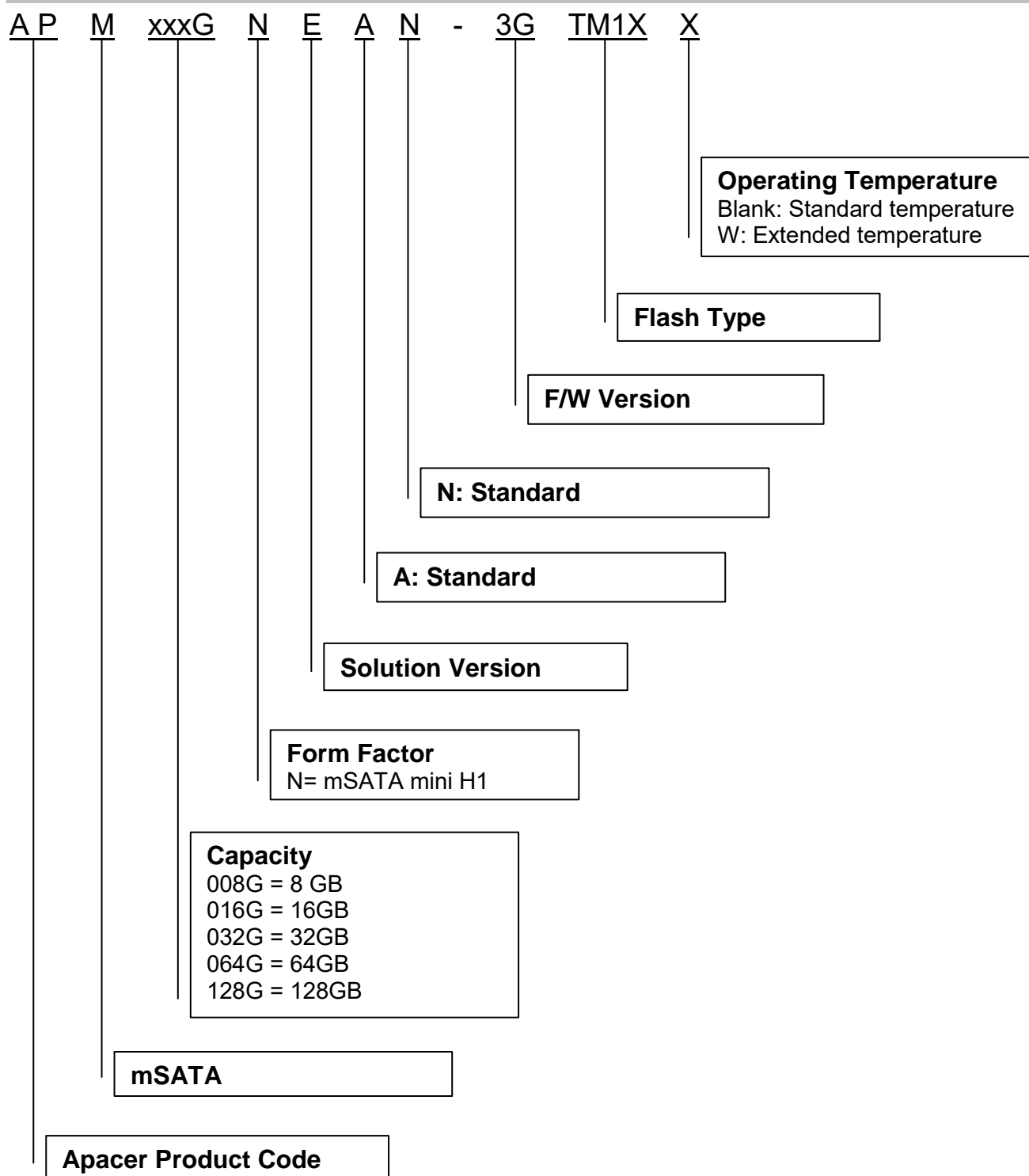
## 6. Mechanical Specifications

### 6.1 Dimensions



## 7. Product Ordering Information

### 7.1 Product Code Designation





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## 7.2 Valid Combinations

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Capacity	Standard Temperature	Extended Temperature
8GB	APM008GNEAN-3GTM1	APM008GNEAN-3GTM1W
16GB	APM016GNEAN-3GTM1	APM016GNEAN-3GTM1W
32GB	APM032GNEAN-3GTM1	APM032GNEAN-3GTM1W
64GB	APM064GNEAN-3GTM1	APM064GNEAN-3GTM1W
128GB	APM128GNEAN-3GTM1G	APM128GNEAN-3GTM1GW

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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## Revision History

Revision	Description	Date
1.0	Official release	11/17/2016
1.1	- Updated performance and power consumption values - Updated product ordering information for 64GB	11/23/2016
1.2	- Added LED Indicators for Drive Behavior on Features page - Added 1.6 LED Indicator Behavior - Updated mechanical specifications	2/8/2017
1.3	Added Thermal Sensor as an optional feature on Features page	2/16/2017

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