RoHS Compliant

Combo SATA Flash Drive

CSD -M Product Specifications

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Version 1.0

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Features:

- **Compliance with SATA Revision 3.1**
  - Serial ATA Revision 3.1
  - SATA 6.0 Gbps interface
  - Backward compatible with SATA 1.5 and 3.0 Gbps interfaces
  - ATA-8 command set
- **Capacities**
  - 128 + 128 GB
  - 256 + 256 GB
- **Performance***
  - Sustained read: up to 470 MB/sec
  - Sustained write: up to 430 MB/sec
  - 4K Random Read: up to 70,000 IOPS
  - 4K Random Write: up to 68,000 IOPS
- **Flash Management**
  - Built-in hardware ECC, enabling up to 40 bit correction per 1K bytes
  - Static/dynamic wear leveling
  - Flash bad-block management
  - S.M.A.R.T.**
  - Power Failure Management
  - ATA Secure Erase**
  - TRIM**
- **NAND Flash Type:** MLC
- **RAID 0 and RAID 1 modes support (requires the support from host system)**
- **Temperature ranges**
  - Operating: 0℃ to 70℃ (32 ~ 158℉)
  - Storage: -40℃ to 100℃ (-40° ~ 212℉)
- **Supply voltage**
  - 5.0 V ± 5%
- **Power consumption (typical)***
  - Active mode: 860 mA
  - Idle mode: 200 mA
- **Form factor**
  - SATA 2.5” drive
  - Dimensions (100.0x69.9x9.3, unit: mm)
- **SAS Connector**
  - 7 + 7-pin SATA signal connector
  - 15-pin SATA power connector
- **Shock & Vibration*****
  - Shock: 1500 G
  - Vibration: 15 G
- **DRAM cache for enhanced random performance**
- **SATA power management**
- **RoHS compliant**

*Based on each drive detected by the host OS. The values addressed here are typical and may vary depending on settings and platforms.
**SMART, TRIM and ATA Secure Erase are NOT executable under RAID modes.
***Non-operating

Table of Contents

1. Product Description

1.1 Introduction

Apacer's CSD (Combo SATA Drive) is a highly powerful combo of dual SATA SSDs created to meet the mission critical demands in today's industrial and embedded computing systems. CSD features two sets of controllers and NAND flash memories, with SAS interface for connection with the host. When installed in computer motherboards, the operating system would detect it as two separate drives so that the host can take advantages of the doubled storage spaces. For instance, one partition may be used as the system boot drive while another can serve as storage.

Regarding the performance, CSD comes with a powerful controller that complies with SATA 6.0 Gbps interface speed and delivers outstanding read/write performance. In addition, CSD also supports RAID 0 (striping mode) and RAID 1 (mirror mode for data backup) modes for sophisticated operations (RAID modes require host system support).

For data efficiency, the internal controlling unit of the CSD is engineered with DRAM for enhanced random performance. In regard of reliability, the drive comes with various firmware implementations including powerful hardware ECC engine, wear leveling, flash block management, S.M.A.R.T., TRIM, and power failure management.

1.2 Capacity Specification

Table 1-1 Capacity specification for each device detected by the OS

Capacity	Total Bytes*	Cylinders	Heads	Sectors	Max LBA*
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192

*Display of total bytes varies from file systems.
**Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

1.3 Performance

Performance of CSD is shown in Table 1-2.

Table 1-2 Performance of each drive detected by the OS

Performance \ Capacity	128 GB	256 GB
Sustained Read (MB/s)	460	470
Sustained Write (MB/s)	295	430
4K Random Read (IOPS)	69,000	70,000
4K Random Write (IOPS)	66,000	68,000

Note: Performance varies from host system settings and flash configurations. IOPS results were measured on 8GB span (16777216 sectors Disk Size), 32 Outstanding I/Os (QD=32), Full Random Data pattern, 4KB Align I/Os and test time was 15minutes.

1.4 Pin Assignments

Table 1-3 describes the CSD SAS connector signal segment, and Table1-4, power segment.

Figure 1-2 SAS Connectors

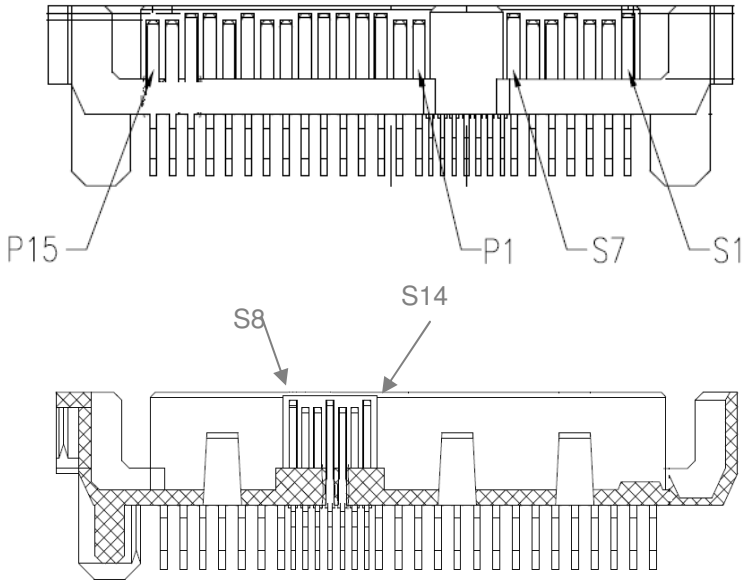


Table 1-3: Signal segment

Pin	Description
S1	Ground
S2	Differential Receive Signal +
S3	Differential Receive Signal -
S4	Ground
S5	Differential Transmit Signal -
S6	Differential Transmit Signal +
S7	Ground

S8	Ground
S9	Differential Receive Signal +
S10	Differential Receive Signal-
S11	Ground
S12	Differential Transmit Signal -
S13	Differential Transmit Signal +
S14	Ground

Table 1-4: Power segment

Pin	Signal/Description
P1	3.3V (unused)
P2	3.3V (unused)
P3	3.3V (unused)
P4	Ground
P5	Ground
P6	Ground
P7	5V
P8	5V
P9	5V
P10	N/C
P11	N/C
P12	Ground
P13	12V (unused)
P14	12V (unused)
P15	12V (unused)

N/C: Non-connected

2. Software Interface

2.1 Command Set

Table 2-1 summarizes the ATA commands supported by CSD.

Table 2-1: Command set

Code	Command	Code	Command
E5h	Check Power Mode	F6h	Security Disable Password
90h	Execute Diagnostics	F3h	Security Erase Prepare
E7h	Flush Cache	F4h	Security Erase Unit
ECh	Identify Device	F5h	Security Freeze Lock
E3h	Idle	F1h	Security Set Password
E1h	Idle Immediate	F2h	Security Unlock
91h	Initialize Device Parameters	7xh	Seek
C8h	Read DMA	EFh	Set Features
25h	Read DMA EXT	C6h	Set Multiple Mode
60h	Read FPDMA Queued	E6h	Sleep
47h	Read Log DMA EXT	B0h	S.M.A.R.T.
2Fh	Read Log EXT	E2h	Standby
C4h	Read Multiple	E0h	Standby Immediate
20 or 21h	Read Sector(s)	CAh	Write DMA
40 or 41h	Read Verify Sector(s)	35h	Write DMA EXT
10h	Recalibrate	61h	Write FPDMA Queued
57h	Write Log DMA EXT	3Fh	Write Log EXT
C5h	Write Multiple	30h or 31h	Write Sector(s)

2.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	Enable/Disable Attribute Autosave
D4h	Execute Off-line Immediate
D5h	Read Log (optional)
D6h	Write Log (optional)
D8h	Enable Operations
D9h	Disable operations
DAh	Return Status

General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status flag
3	Value
4	Worst
5*-11	Raw Data

*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on hours
12 (0x0C)	Power cycle count
163 (0xA3)	Max. erase count
164 (0xA4)	Avg. erase count
166 (0xA6)	Total later bad block count
167 (0xA7)	SSD Protect Mode (vendor specific)
168 (0xA8)	SATA PHY Error Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
241 (0xF1)	Total sectors of write

Notes: SMART is NOT executable under RAID modes.

3. Flash Management

3.1 Error Correction/Detection

CSD implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 40 bits error in 1K bytes.

3.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

3.3 Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

3.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

3.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

Notes: ATA Secure Erase is NOT executable under RAID modes.

3.6 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller whick blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

Notes: ATA Secure Erase is NOT executable under RAID modes.

3.7 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 µs (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.

Note: the behaviors of power management features would depend on host/device settings.

4. Environment Specifications

4.1 Environmental

CSD environmental specifications follow the US Military Standard MIL-STD-810F, as shown in the following table.

Table 4-1 SFD18S4-M environmental specifications

Environment	Specification
Temperature	0℃ to 70℃ (Operating)
	-40℃ to 100℃ (Non-operating)
Vibration	Non-operating : Sine wave, 15(G), 10~2000(Hz), Operating : Random, 7.69(Grms), 20~2000(Hz)
Shock	Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms

4.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in CSD drive. The prediction result for the CSD is more than 1,000,000 hours.

Notes about the MTBF:

The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

4.3 Certification and Compliance

CSD complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810F

5. Electrical Characteristics

5.1 Operating Voltage

Table 5-1 lists the supply voltage for CSD.

Table 5-1 CSD operating voltage

Parameter	Conditions
Supply voltage	5V ±5% (4.75-5.25 V)

5.2 Power Consumption

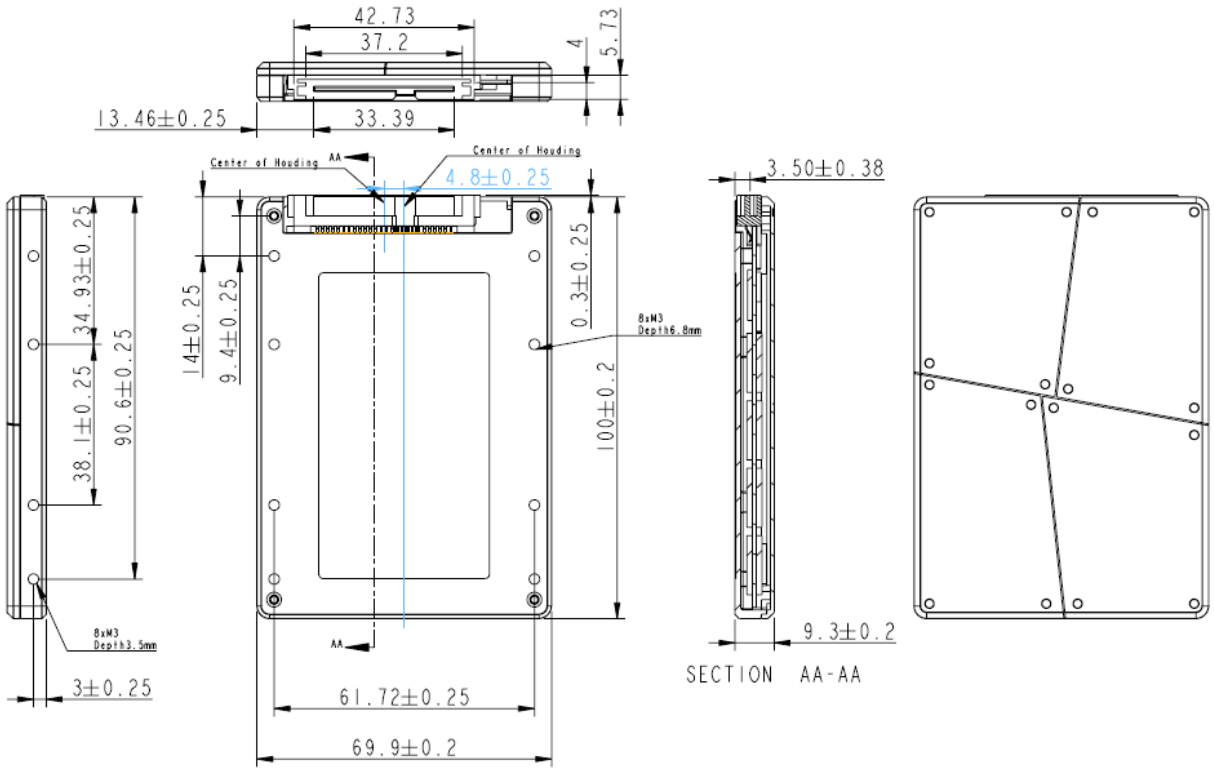
Table 5-2 Power consumption (typical) of each device detected by the OS

Mode \ Capacity	128 GB	256 GB
Active (mA)	610	860
Idle (mA)	170	200

Note: Power consumptions may vary depending on settings and platforms.

6. Physical Characteristics

6.1 Dimensions



Unit: mm
Tolerance: ± 0.2

7. Product Ordering Information

7.1 Product Code Designations

A P CSD 7 x x x x – A XX X

Temperature Range
Blank: Standard
W: Extended Temperature

Flash Type
TM: Toshiba MLC

Version Control

Capacities:

256G	256 GB
512G	512GB

Solution version

Combo SATA Drive

Apacer Product Code

7.2 Valid Combinations

Capacity	Standard
256 GB	APCSD7256G-ATM
512 GB	APCSD7512G-ATM

Note:
1. Please consult with Apacer sales representative for availability.
2. **Capacities specified in the Product Ordering Information indicate the total of the dual SATA drives.**

Revision History

Revision	Description	Date
0.1	Preliminary release	07/01/2013
0.2	Updated performance and power consumption Updated pin assignments	07/15/2013
0.3	Added Product Ordering Information	08/08/2013
0.4	Updated the address of Taiwan headquarter Removed the block diagram	08/14/2013
1.0	Official release	03/05/2014

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