

Apacer Micro SATA Disk Chip

uSDC-Plus Design Guide

October 20, 2015

Version 2.3



Apacer Technology Inc.

1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

www.apacer.com

Table of Contents

1. General Description	2
2. Features	2
3. Pin Definitions	3
4. SATA Trace Management.....	8
5. Power Domain	9
5.1 Power Supply	9
5.2 Power-on Sequence	11
5.2.1 Adjustable POR function: (optional function)	12
5.3 Decoupling Requirements.....	13
5.4 Ferrite Chip Bead Requirements	14
5.5 Device Sleep	14
5.6 DAS	15
6. Crystal	16
7. Debug Use	16
8. GPIO	16
9. uSDC Power Current & Circuit	17
10. Reference – Overview.....	19
11. Reference BOM List.....	21

1. General Description

Apacer uSDC (Micro SATA Disk Chip) is a presentation of revolutionary breakthrough to NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed SATA 6.0 Gbps interface in an embedded BGA form factor, compliant with JEDEC MO-276. Micro SATA Disk Chip is currently the tiniest storage solution at present, with controller and NAND flash embedded inside. Though micro in size, the uSDC can provide moderate capacity and outstanding performance, ideal as operating system boot drive for compact embedded systems. With its micro-size and ultra speed, the uSDC is definitely the ideal storage solution for high performance demand mobile devices.

The following sections will provide brief instructions for the circuit/layout design for this storage solution.

2. Features

Support SATA 6.0 Gbps Interface

- Compliant with SATA 6.0 Gbps
- Support power management

Operation Voltage Supply

- 3.3V: 3.135V ~ 3.465V
- 1.8V: 1.71V ~ 1.89V
- 1.2V: 1.14V ~ 1.26V

Power Saving Implementation

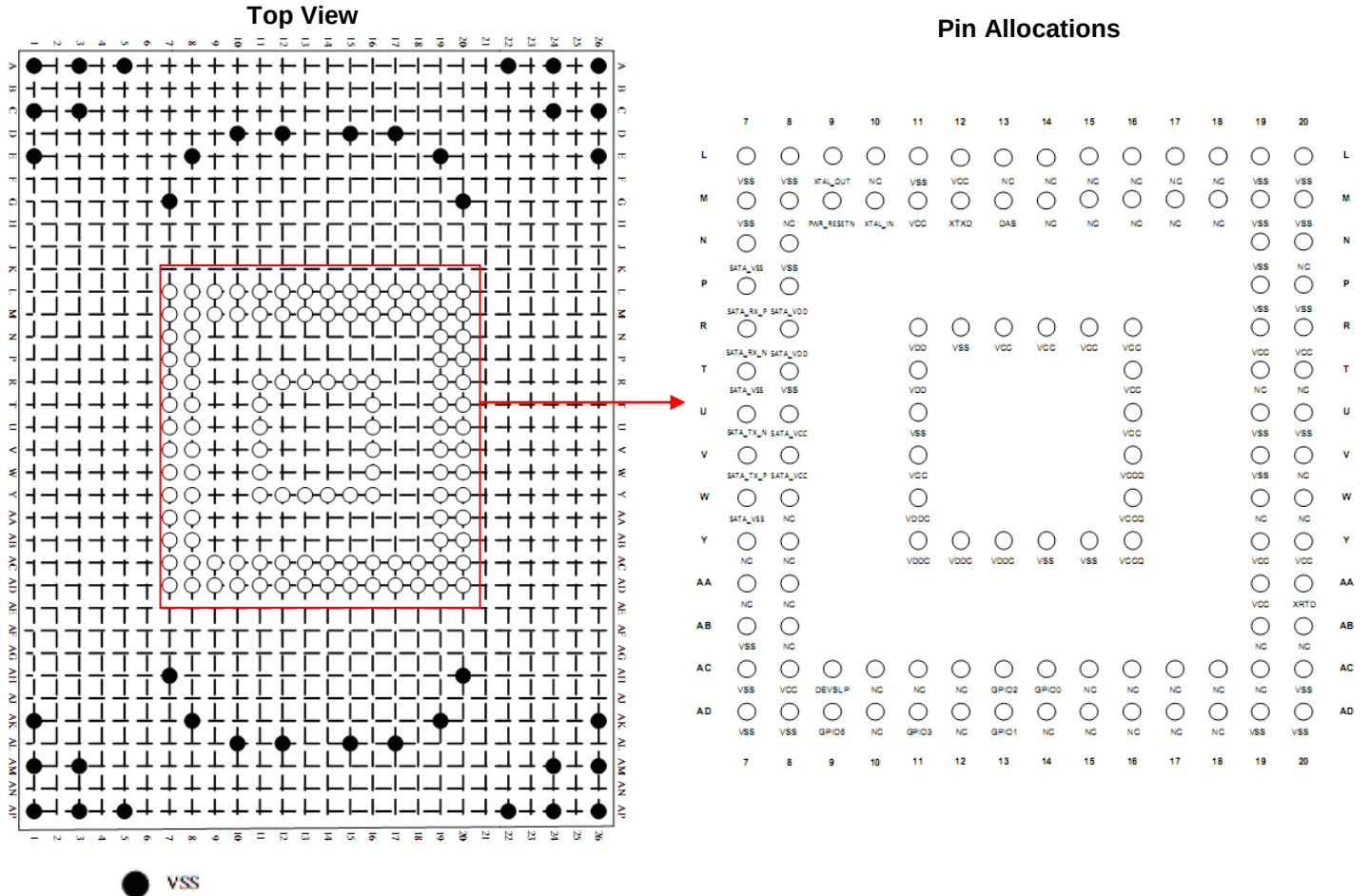
- Idle mode
- Sleep mode
- Partial mode
- Slumber mode
- Device sleep mode

Built-in 32-Bit Microcontroller (Core)

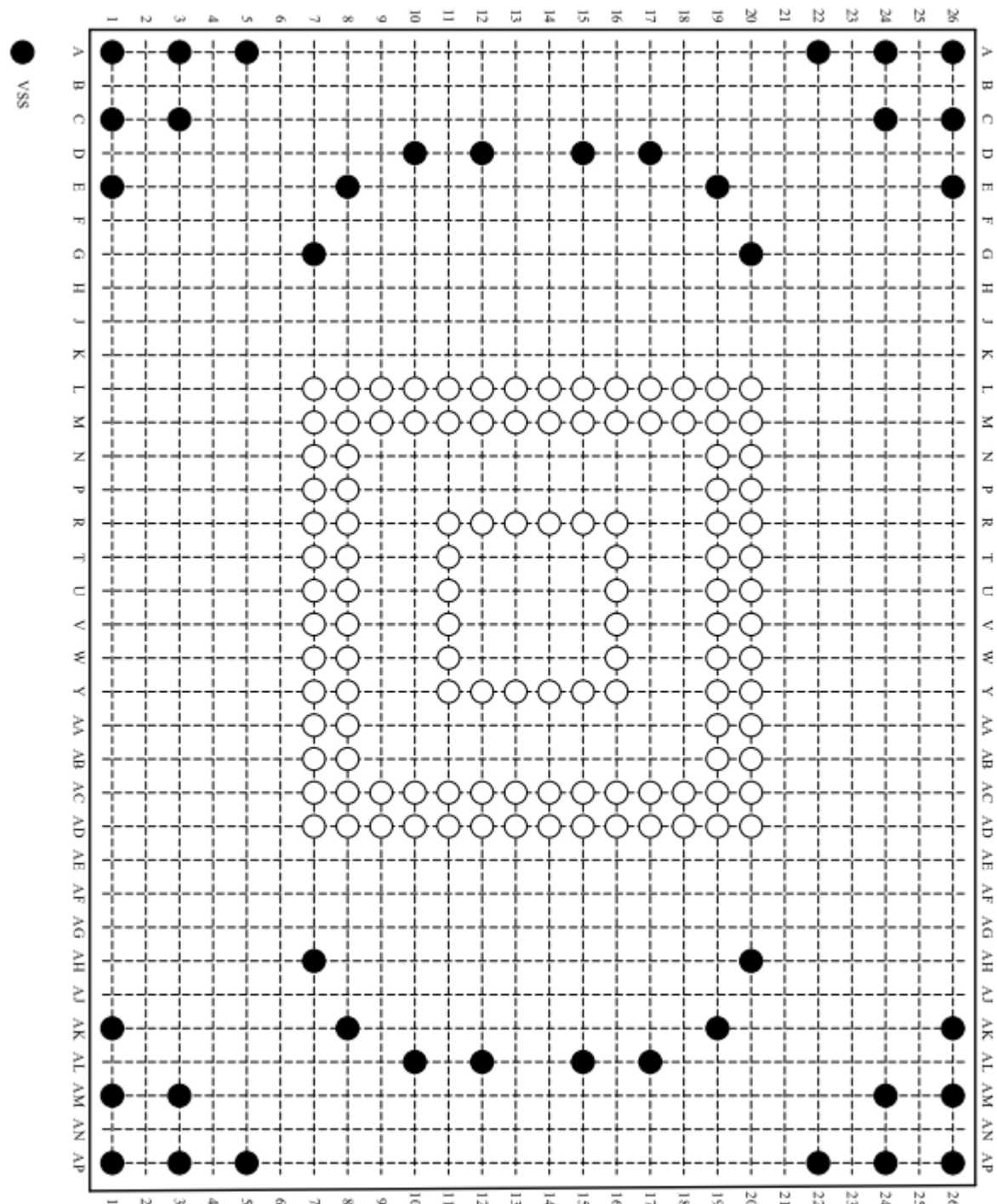
UART function

Implement Voltage Detector

3. Pin Definitions



Top View (enlarged image)



Pin Allocations (enlarged image)

	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
L	○	○	○	○	○	○	○	○	○	○	○	○	○	○	L
	VSS	VSS	XTAL_OUT	NC	VSS	VCC	NC	NC	NC	NC	NC	NC	VSS	VSS	
M	○	○	○	○	○	○	○	○	○	○	○	○	○	○	M
	VSS	NC	PWR_RESETN	XTAL_IN	VCC	XTXD	DAS	NC	NC	NC	NC	NC	VSS	VSS	
N	○	○											○	○	N
	SATA_VSS	VSS											VSS	NC	
P	○	○											○	○	P
	SATA_RX_P	SATA_VDD											VSS	VSS	
R	○	○			○	○	○	○	○	○			○	○	R
	SATA_RX_N	SATA_VDD			VDD	VSS	VCC	VCC	VCC	VCC			VCC	VCC	
T	○	○			○					○			○	○	T
	SATA_VSS	VSS			VDD					VCC			NC	NC	
U	○	○			○					○			○	○	U
	SATA_TX_N	SATA_VCC			VSS					VCC			VSS	VSS	
V	○	○			○					○			○	○	V
	SATA_TX_P	SATA_VCC			VCC					VCCQ			VSS	NC	
W	○	○			○					○			○	○	W
	SATA_VSS	NC			VDDC					VCCQ			NC	NC	
Y	○	○			○	○	○	○	○	○			○	○	Y
	NC	NC			VDDC	VDDC	VDDC	VSS	VSS	VCCQ			VCC	VCC	
AA	○	○											○	○	AA
	NC	NC											VCC	XRTD	
AB	○	○											○	○	AB
	VSS	NC											NC	NC	
AC	○	○	○	○	○	○	○	○	○	○	○	○	○	○	AC
	VSS	VCC	DEVSLP	NC	NC	NC	GPIO2	GPIO0	NC	NC	NC	NC	NC	VSS	
AD	○	○	○	○	○	○	○	○	○	○	○	○	○	○	AD
	VSS	VSS	GPIO6	NC	GPIO3	NC	GPIO1	NC	NC	NC	NC	NC	VSS	VSS	
	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Description

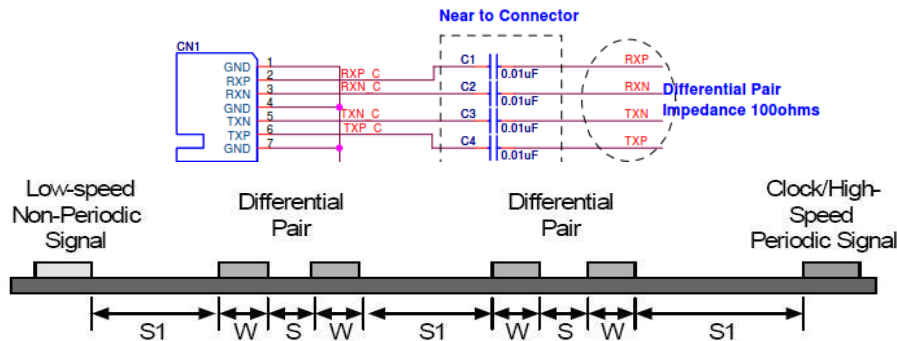
Name (Bottom view)	BGA156 (Top view)	Type (I/O)	Description
UART/GPIO			
XTXD	M12	O	UART transmit/receive port (For Apacer internal debug use)
XRXD	AA20	I	
GPIO0*	AC14	IO	General purpose input/output pins
GPIO1*	AD13		
GPIO6*	AD9		
GPIO2*	AC13	IO	VA – Write Protect
GPIO3*	AD11	IO	VA – Erase
SATA_RX_N SATA_RX_P	R7 P7	I	Differential signal pair A. SATA device receive signal differential pair
SATA_TX_N SATA_TX_P	U7 V7	O	Differential signal pair B. SATA device transmit signal differential pair
DAS	M13	O	Device activity signal
SATA_VCC	U8, V8		+3.3V
SATA_VDD	P8, R8		+1.2V
SATA_VSS	N7, T7, W7		Ground
Control Signals			
XTAL_IN XTAL_OUT	M10 L9	I O	Crystal input/output pin (40MHz)
PWR_RESETN	M9	I	Hardware reset, low active
Power Supply Signals			
VCC	L12, M11, R13, R14, R15, R16, R19, R20, T16, U16, V11, Y19, Y20, AA19, AC8		+3.3V
VDDC	W11, Y11, Y12, Y13		+1.2V
VCCQ	V16, W16, Y16		+1.8V
VDD	R11, T11		+1.2V for PLL
GND Signals			
VSS	R12, U11, L7, L8, M7, L11, L19, L20, M19, M20, N19, P19, AC20, AD20, AD19, AD8, T8, Y14, Y15, U19, P20, U20, V19, AC7, AB7, N8, A1, C1, E1, AK1, AM1		Ground
VSS	AP1, A3, C3, AM3, AP3, A5, AP5, G7, AH7, E8, AK8, D10,		Ground

uSDC Design Guide

	AL10, D12, AL12, D15, AL15, D17, AL17, E19, AK19, G20, AH20, A22, AP22, A24, C24, AM24, AP24, A26, C26, E26, AK26, AM26, AP26		
Other Signals			
DEVSLP	AC9	I	Device Sleep
NC	AA7, AB19, AB20, AB8, AC10, AC11, AC15, AC16, AC17, AC18, AC19, AD10, AD12, AD14, AD15, AD16, AD17, AD18, L10, M16, M17, M8, T19, T20, W19, W8, Y7, Y8, L13, L14, M14, M15, M18, N20, V20, W20, AC12		DNU
Debug	L15, L16, L17, L18, AA8, AD7		For Apacer internal debug use (AD7- Standard definition : VSS Apacer definition : for debug)

*The GPIO pins are non-connected by default. For specific configurations for the GPIO pins, such as Apacer Security Features, please consult with Apacer product managers or sales representatives for further details.

4. SATA Trace Management



Impedance level: Differential: $100\Omega \pm 5\%$, Single End: $50\Omega \pm 5\%$, Ground Referencing

SATA Trace Width and Separation: $W/S/W = 6/14.2/6$, $S1 = 20$ mil
(may vary from PCB structure, but impedance must remain)

Signals	Differential Impedance	Single End	Width	Length	Length matching within differential pair	Space to others (S1)
Tx +/- Rx +/-	$100\Omega \pm 5\%$, Ground Referencing	$50\Omega \pm 5\%$, Ground Referencing	$6/14.2/6$ – mil routing	$<2"$	± 5 mils	20 mils

SATA AC Coupling Requirements

Signals	Cap Value	Quantity	Note
Tx +/- Rx +/-	0402 Size 10nF/X7R/ $\pm 10\%$	4	Place cap(s) near Host

- Each differential pair should be matched in length (allowable tolerance ± 5 mil)
- The width separation is based on PCB impedance (total $100\Omega \pm 5\%$).
- The length of the differential pairs shall be as close as possible to the connector, must be less than 2 inches.
- There shall be no stubs (test pins) on these traces.
- All angles among traces shall be greater or equal to 135 degrees.
- SATA signals must be reference ground plane.
- The whole SATA traces must be on the same plane and no interruption is allowed (any discontinuity occurred to the trace or split ground plane will lead to signal integrity problems)
- Do not change the layout layers frequently. It will cause signal problems.
- Do not route SATA traces under connectors, oscillation source, magnetic devices or sensitive coupling loops.
- Clocks and other high-speed periodic signals shall be kept away from SATA signal pairs.
- The SATA connector golden fingers must be kept un-referenced.

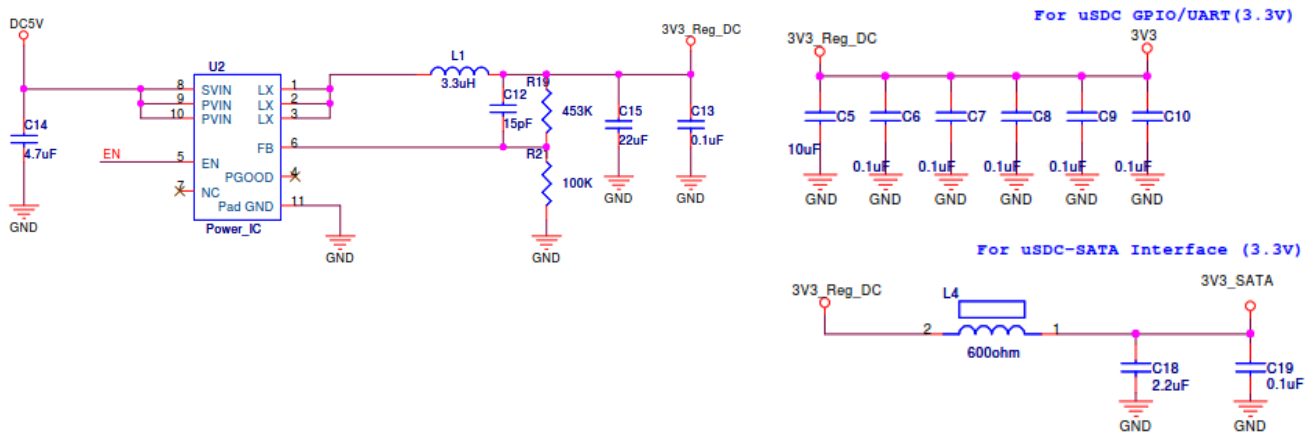
5. Power Domain

5.1 Power Supply

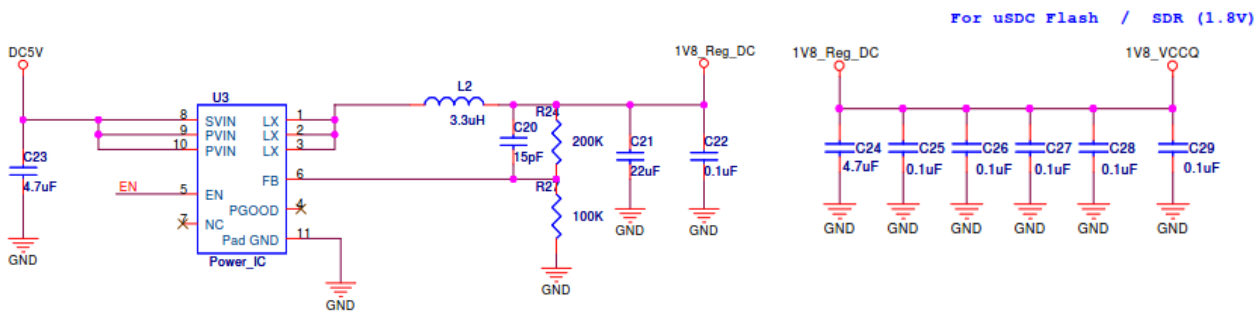
The uSDC comes with 3 levels of voltage requirements: 3.3V, 1.8V and 1.2V. The following table indicates the required power supply and the ranges.

Parameter	Descriptions	Min.	Typical	Max.	Unit
Input Voltage	SATA & NAND Flash	+3.135	+3.3	+3.465	V
	NAND Flash I/O & SDR	+1.71	+1.8	+1.89	V
	Controller core supply	+1.14	+1.2	+1.26	V

+3V3 Controller Circuit, +3V3_SATA Controller Circuit



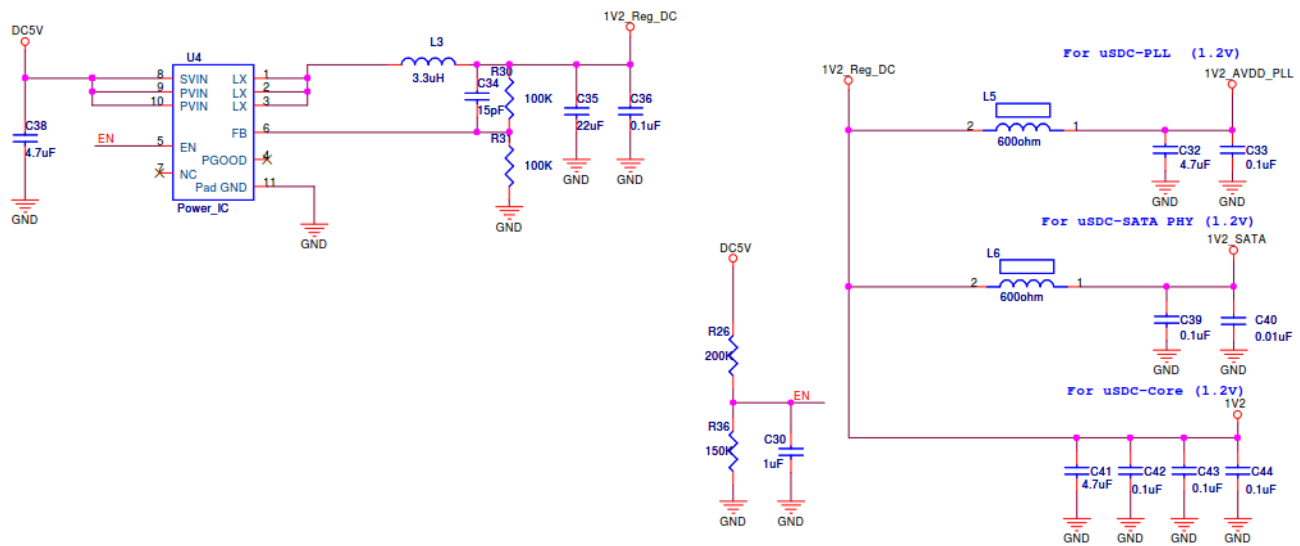
+1V8_VCCQ Controller Circuit



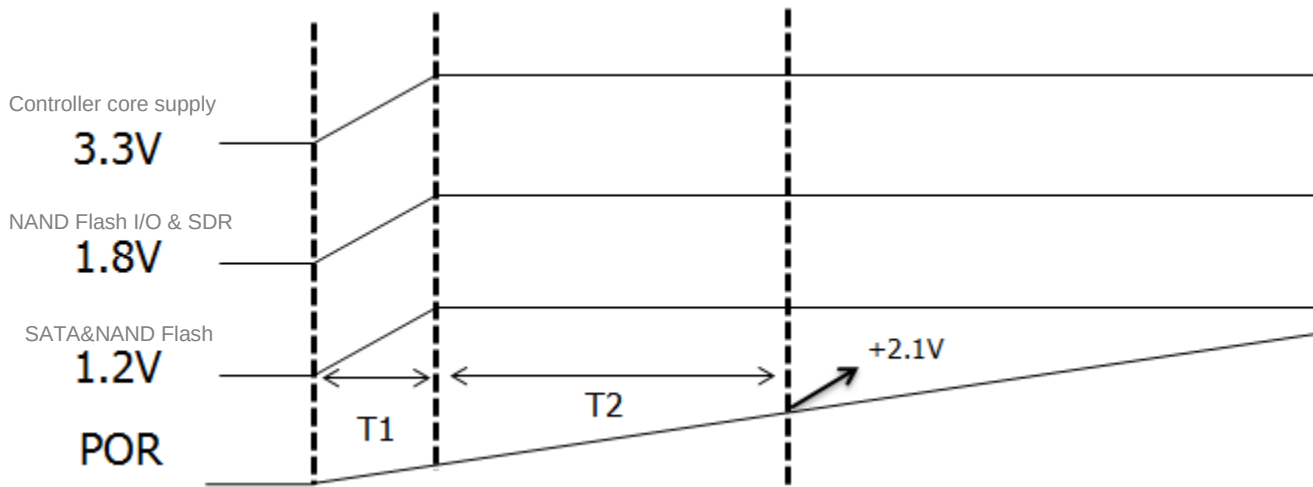
uSDC Design Guide



+1V2_AVDD_PLL, +1V2_SATA, and +1V2 Controller Circuit



5.2 Power-on Sequence

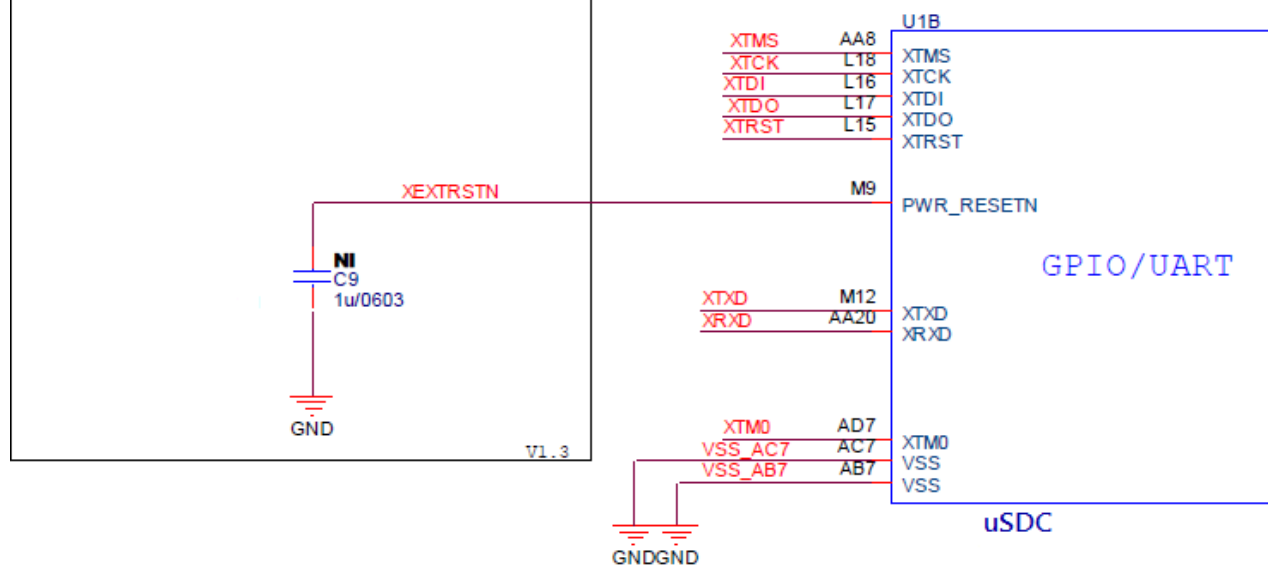


Parameter	Min	Nom	Max.	Unit
Power Ready(T1)	-	-	1	ms
POR Ready (T2)	10	-	100	ms

Note:

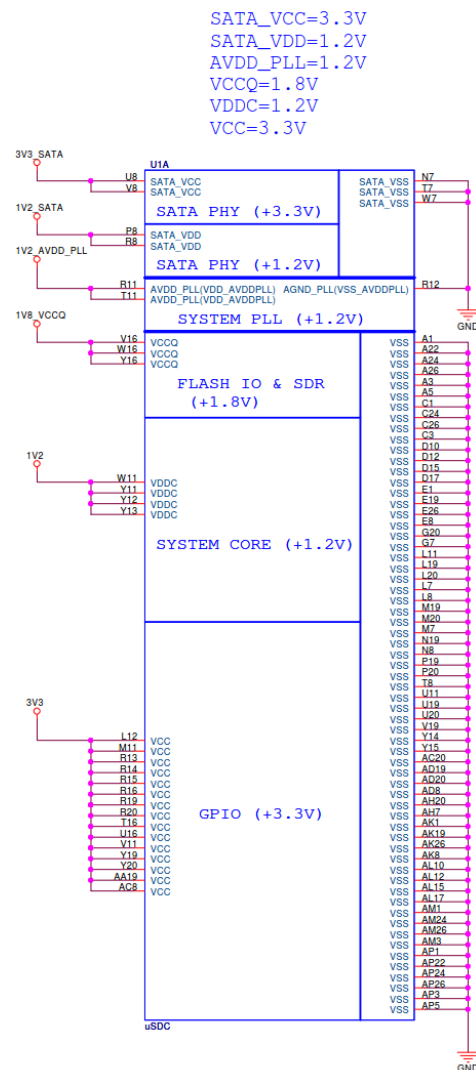
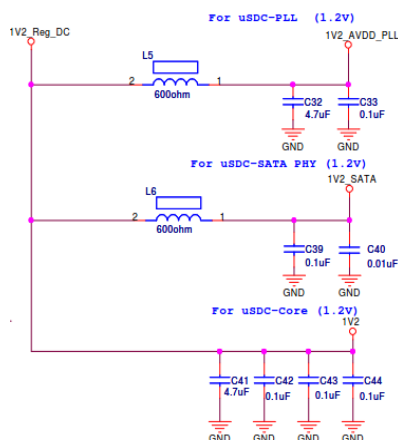
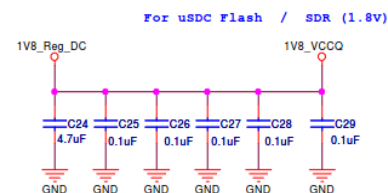
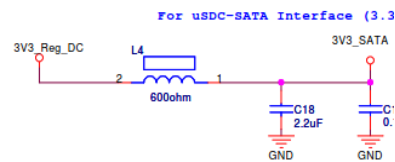
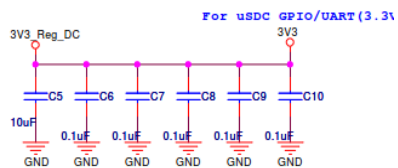
1. Internal POR Vih=2.1V.
2. The currents among 3.3v/1.8v/1.2v make no difference in sequence. The only key factor is that they must achieve those voltage levels under 1ms.
3. When reset signal keep in high, the uSDC will start working.

Component	Voltage	Qty	Note
C9	6.3V (Min)	1	1. Close to uSDC controller 2. Per adding 1uF delay 11ms 3. POR delay time is up to 100ms.



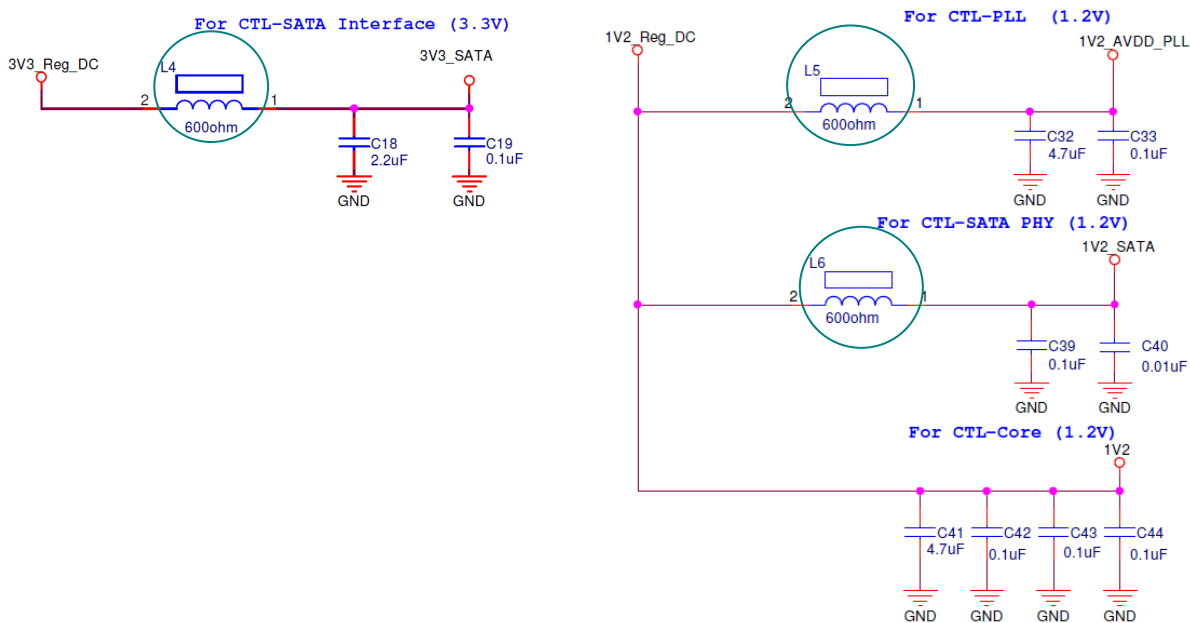
5.3 Decoupling Requirements

Voltage Plane Name	Supply (volts typical)	Cap value (6.3V min rating)	Qty	Place cap(s) near ball(s)
+1V2_AVDD_PLL	+1.2V	4.7uF 0.1uF	1 1	R11, T11
+1V2_SATA	+1.2V	0.1uF 10nF	1 1	P8, R8
+1V2	+1.2V	0.1uF 4.7uF	3 1	W11, Y11, Y12, Y13
+1V8_VCCQ	+1.8V	0.1uF 4.7uF	5 1	V16, W16, Y16
+3V3	+3.3V	0.1uF 10uF	5 1	L12, M11, R13, R14, R15, R16, R19, R20, T16, U16, V11, Y19, Y20, AA19, AC8
+3V3_SATA	+3.3V	0.1uF 2.2uF	1 1	U8, V8



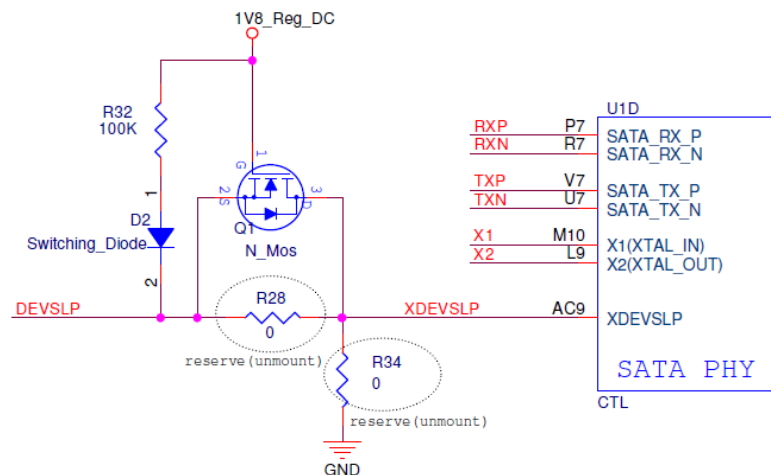
5.4 Ferrite Chip Bead Requirements

Voltage Plane Name	Supply (volts typical)	Value	DC Resistance Max. (m Ω)	Qty	Place cap(s) near ball(s)
+1V2_AVDD_PLL	+1.2V	0603/600 Ω /2A	150	1	R11, T11
+1V2_SATA	+1.2V	0603/600 Ω /2A	150	1	P8, R8
+3V3_SATA	+3.3V	0603/600 Ω /2A	150	1	U8, V8



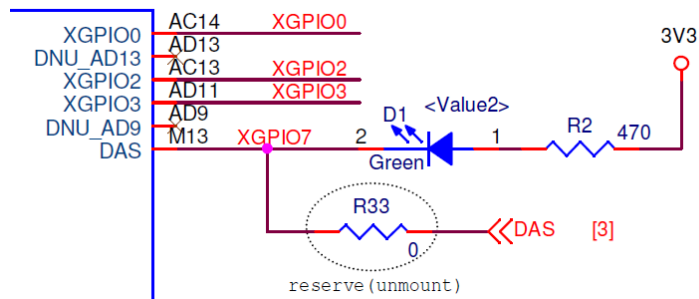
5.5 Device Sleep

The uSDC supports Device Sleep (DevSLP or DevSleep) and this feature is included in the hardware design.



5.6 DAS

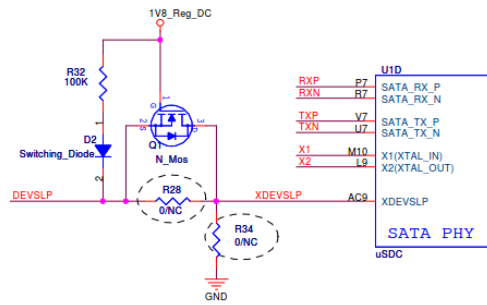
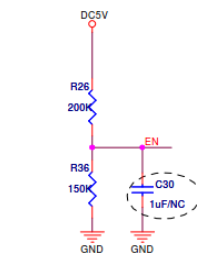
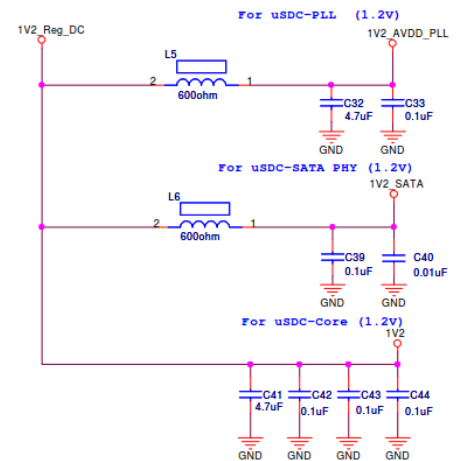
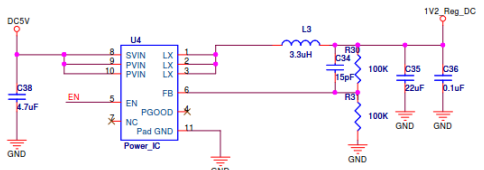
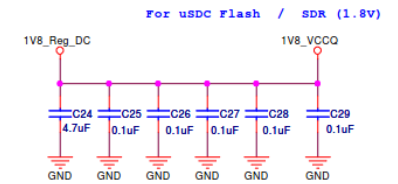
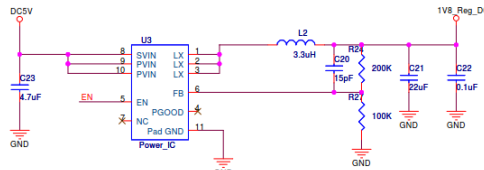
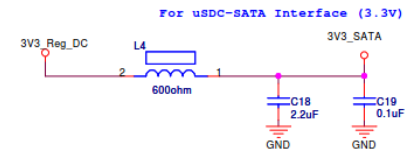
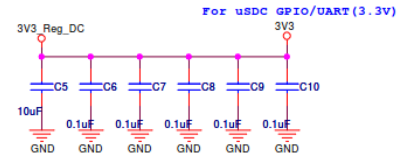
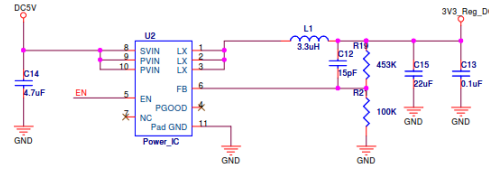
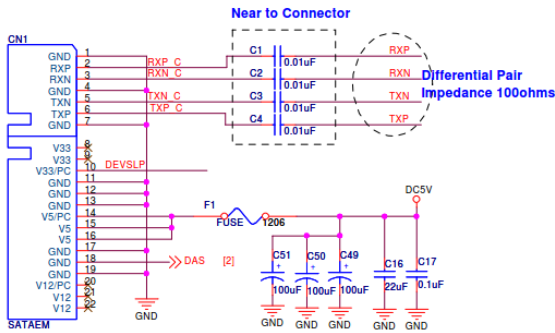
The uSDC supports DAS (Device Activity Signal) usage. At low impedance, it indicates that the device is active. To pull high, it requires 3.3V.



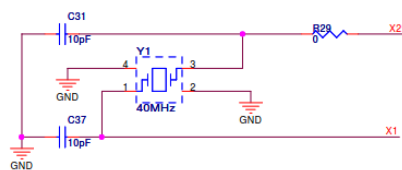
Apacer
Access the best

Rev. 2.3

uSDC Design Guide



Note :
NC= reserve (unmount)



11. Reference BOM List

Item Number	Part Reference	Q'ty	Description1
1	C1,C2,C3,C4,C40	5	Cap 0.01uF
2	C5	1	Cap 10uF
3	C6,C7,C8,C9,C10,C13,C17,C19,C22,C25,C26,C27,C28,C29,C33,C36,C39,C42,C43,C44	20	Cap 0.1uF
4	C12,C20,C34	3	Cap 15pF
5	C14,C23,C24,C32,C38,C41	6	Cap 4.7uF
6	C15,C16,C21,C35	4	Cap 22uF
7	C18	1	Cap 2.2uF
8	C31,C37	2	Cap 10pF
9	C49,C50,C51	3	TanCap 100uF
10	CN1	1	SATA Conn. 7+15pin
11	D1	1	LED
12	D2	1	Switching Diode CDSF355B
13	F1	1	Fuse
14	L1,L2,L3	3	L=3.3uH
15	L4,L5,L6	3	BEAD 600ohm
16	Q1	1	Power MOSFET N-ch SM2326NSAN
17	R2	1	Res 470ohm
18	R21,R27,R30,R31,R32	5	Res 100Kohm
19	R19	1	Res 453Kohm
20	R24,R26	2	Res 200Kohm
21	R4,R11*,R14*, R29	2	Res 0ohm
22	R36	1	Res 150Kohm
23	U1	1	uSDC
24	U2,U3,U4	3	Step-Down Converter
25	Y1	1	Crystal 40MHz

* R11, R14: necessary for GPIO2 and GPIO3 VA function

Revision History

Revision	Date	Description	Remark
0.1	03/26/2013	Preliminary	
0.2	04/03/2013	Model name changed to uSDC (Micro SATA Disk Chip)	
1.0	11/01/2013	Official release	
1.1	12/18/2013	Updated the power-on sequence diagram and added notes for further details	
1.2	01/20/2014	Added Device Sleep back into the document due to firmware upgrade	
1.3	07/10/2014	Added "Reference Schematic"	
1.4	07/15/2014	Modified the "Reference Overview" section Removed "Testing Board" section	
1.5	07/21/2014	Added Reference BOM List	
1.6	08/08/2014	Updated power sequence Revised reference schematic	
1.7	09/03/2014	Added "uSDC Power Current & Circuit" section Simplified description for Device Sleep in Pin Assignment section Revised schematics	
1.8	09/10/2014	Images clearness re-do	
1.9	10/06/2014	Updated BOM list Added "L18" into "NC" in pin assignment Updated the reference schematics	
1.91	12/18/2014	Updated Power-on Sequence.	
1.91e	12/18/2014	Updated alternative POR values.	
2.0	06/17/2015	Updated pin definition of section 7: L15(XTRST), L16(XTDI), L17(XTDO), L18(XTCK), AA8(XTMS), AD7(XTM0) are for Apacer internal debug use.	
2.1	09/14/2015	Re-defined 5.2 power on sequence timing	
2.2	10/15/2015	Revised name definition : GPIO4->GPIO3 for VA – Write Protect feature GPIO2 for VA – Erase feature Added section 8 – GPIO Revised 5.2.1 , POR delay time is up to 120ms Modified reference BOM list :added R11,R14	
2.3	10/20/2015	Added VA trigger condition table in section 8	

Global Presence

Taiwan (Headquarters)	Apacer Technology Inc. 1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan R.O.C. Tel: 886-2-2267-8000 Fax: 886-2-2267-2261 amtsales@apacer.com
U.S.A.	Apacer Memory America, Inc. 46732 Lakeview Blvd., Fremont, CA 94538 Tel: 1-408-518-8699 Fax: 1-510-249-9568 sa@apacerus.com
Japan	Apacer Technology Corp. 5F, Matsura Bldg., Shiba, Minato-Ku Tokyo, 105-0014, Japan Tel: 81-3-5419-2668 Fax: 81-3-5419-0018 jpservices@apacer.com
Europe	Apacer Technology B.V. Science Park Eindhoven 5051 5692 EB Son, The Netherlands Tel: 31-40-267-0000 Fax: 31-40-267-0000#6199 sales@apacer.nl
China	Apacer Electronic (Shanghai) Co., Ltd Room D,22/FL,No2,Lane600,JieyunPlaza, Tianshan RD,Shanghai,200051,China Tel: 86-21-6228-9939 Fax: 86-21-6228-9936 sales@apacer.com.cn
India	Apacer Technologies Pvt Ltd Unit No.201, "Brigade Corner", 7th Block Jayanagar, Yediyur Circle, Bangalore – 560082, INDIA. Tel: +91-80-4152-9061/62/63 Fax:+91-80-4170-0215 sales_india@apacer.com