RoHS Compliant

Micro SATA Disk Chip

uSDC-M Plus Specifications

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Version 2.0

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Features:

- **Standard Serial ATA Interface**
  - SATA 6.0 Gbps interface compliance
  - ATA-compatible command set
- **Capacities**
  - 8, 16, 32, 64 GB
- **Performance***
  - Sustained read: up to 510 MB/sec
  - Sustained write: up to 180 MB/sec
  - Random read 4K: up to 39,000 IOPS
  - Random write 4K: up to 12,000 IOPS
- **Flash Management**
  - Supports ECC up to 72 bit correction per 1K Byte data
  - Wear leveling
  - Flash bad-block management
  - S.M.A.R.T.
  - Power Failure Management
  - ATA Secure Erase
  - TRIM
- **NAND Flash Type:** MLC
- **Temperature ranges**
  - Operating
    Standard: 0°C to 70°C
    Extended: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Supply voltage**
  - 3.3V ± 5%
  - 1.8V ± 5%
  - 1.2V ± 5%
- **Power consumption (typical)***
  - Active mode : 445 mA
  - Idle mode : 90 mA
- **SATA Power Management**
  - Partial mode
  - Slumber mode
  - Device Sleep mode
- **Package**
  - 16 x 20 x 1.4, unit : mm
  - 156 Ball
- **Form Factor**
  - JEDEC MO-276
- **RoHS compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

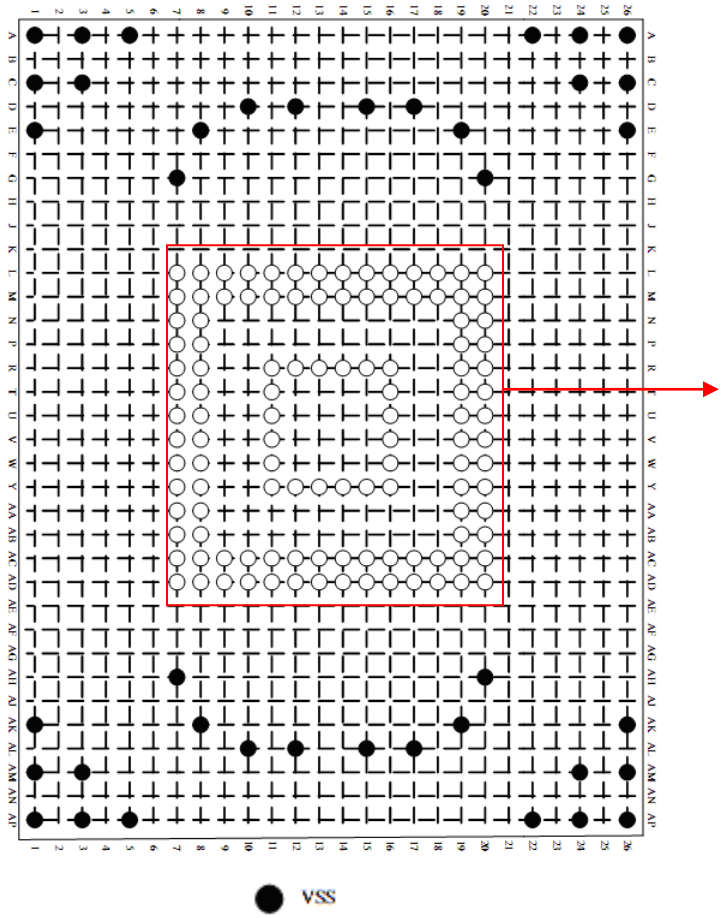
Table of Contents

1. General Description

Apacer Micro SDC (Micro SATA Disk Chip,uSDC) presents a revolutionary breakthrough of NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed SATA 6.0 Gbps interface in an embedded BGA form factor, compatible with JEDEC MO-276. Formed in a size of an IC chip, the speedy uSDC can offer up to 64GB in capacity and the performance level can reach up to 510 MB/s for read and 180 MB/s for write. With its micro-size and ultra speed, the uSDC is definitely the ideal storage solution for high performance demand mobile devices.

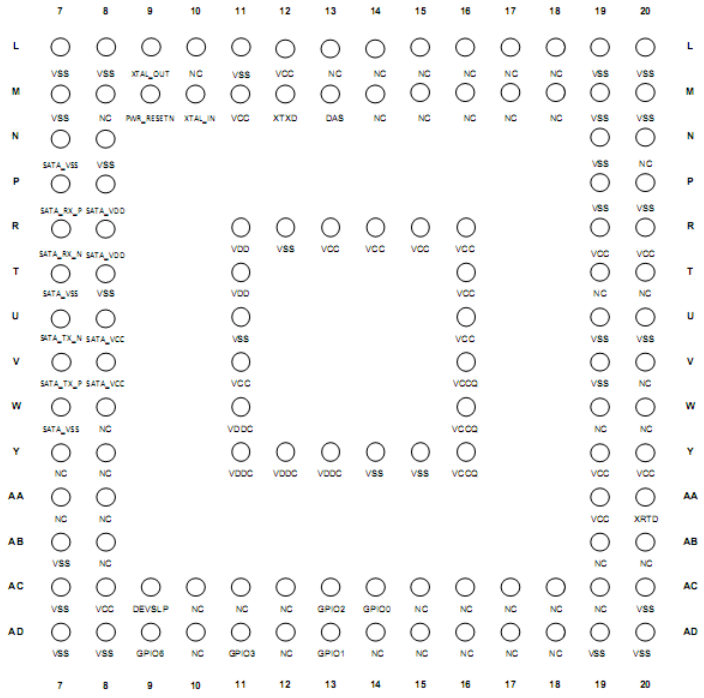
2. Pin Assignments

Top View

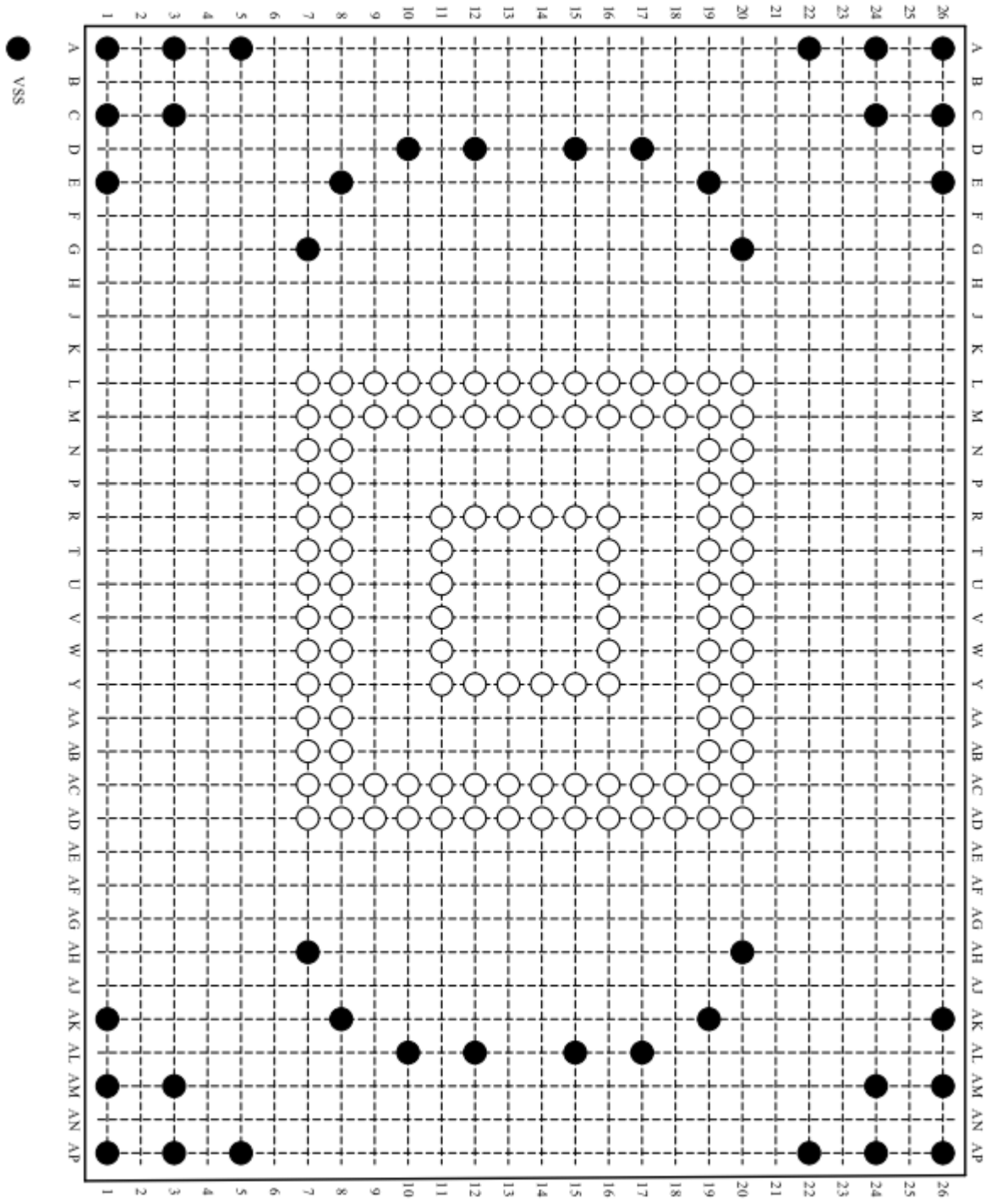


VSS

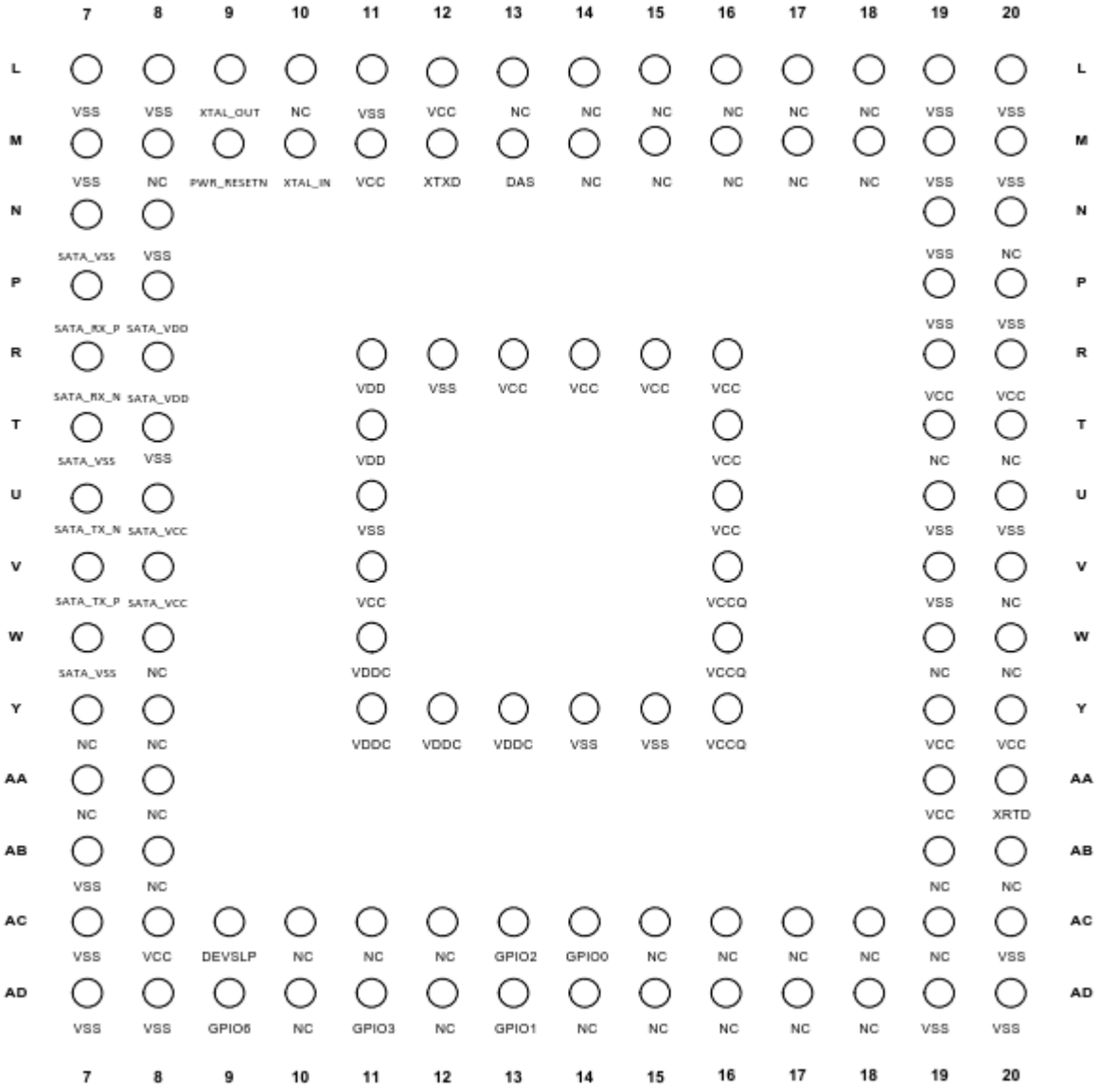
Pin Allocations



Top View (enlarged image)



Pin Allocations (enlarged image)



Pin Description

Name (Bottom view)	BGA156 (Top view)	Type (I/O)	Description
UART/GPIO			
XTXD XRXD	M12 AA20	O I	UART transmit/receive port (For Apacer internal debug use)
GPIO0*	AC14	IO	General purpose input/output pins
GPIO1*	AD13		
GPIO2*	AC13		
GPIO3*	AD11		
GPIO6*	AD9		
SATA_RX_N SATA_RX_P	R7 P7	I	Differential signal pair A. SATA device receive signal differential pair
SATA_TX_N SATA_TX_P	U7 V7	O	Differential signal pair B. SATA device transmit signal differential pair
DAS	M13	O	Device activity signal
SATA_VCC	U8, V8		+3.3V
SATA_VDD	P8, R8		+1.2V
SATA_VSS	N7, T7, W7		Ground
Control Signals			
XTAL_IN XTAL_OUT	M10 L9	I O	Crystal input/output pin (40MHz)
PWR_RESETN	M9	I	Hardware reset, low active
Power Supply Signals			
VCC	L12, M11, R13, R14, R15, R16, R19, R20, T16, U16, V11, Y19, Y20, AA19, AC8		+3.3V
VDDC	W11, Y11, Y12, Y13		+1.2V
VCCQ	V16, W16, Y16		+1.8V
VDD	R11, T11		+1.2V for PLL
GND Signals			
VSS	R12, U11, L7, L8, M7, L11, L19, L20, M19, M20, N19, P19, AC20, AD20, AD19, AD8, T8, Y14, Y15, U19, P20, U20, V19, AC7, AB7, N8, A1, C1, E1, AK1, AM1		Ground
VSS	AP1, A3, C3, AM3, AP3, A5,		Ground

	AP5, G7, AH7, E8, AK8, D10, AL10, D12, AL12, D15, AL15, D17, AL17, E19, AK19, G20, AH20, A22, AP22, A24, C24, AM24, AP24, A26, C26, E26, AK26, AM26, AP26		
Other Signals			
DEVSLP	AC9	I	Device Sleep
NC	AA7, AB19, AB20, AB8, AC10, AC11, AC15, AC16, AC17, AC18, AC19, AD10, AD12, AD14, AD15, AD16, AD17, AD18, L10, M16, M17, M8, T19, T20, W19, W8, Y7, Y8, L13, L14, M14, M15, M18, N20, V20, W20, AC12		DNU
DEBUG	L15, L16, L17, L18, AA8, AD7		For Apacer internal debug use (AD7- Standard definition : VSS Apacer definition : for dubug)

*The GPIO pins are non-connected by default. For specific configurations for the GPIO pins, such as Apacer Security Features, please consult with Apacer product managers or sales representatives for further details.

3. Product Specifications

3.1 Capacity

Table 3-1: Capacity specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
8 GB	8,012,390,400	15,525	16	63	15,649,200
16 GB	16,013,942,784	16,383	16	63	31,277,232
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424

*Display of total bytes varies from file systems.
**Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

3.2 Performance

Table 3-2: Performance

Capacity / Performance	8 GB	16 GB	32 GB	64 GB
Sustained read (MB/s)	145	290	510	510
Sustained write (MB/s)	45	80	150	180
Random Read (IOPS)	17,000	22,000	23,000	39,000
Random Write (IOPS)	1,000	3,000	5,000	12,000

Note:
Results may differ from various flash configurations or host system settings.
IOPS results were measured on 8GB span (16777216 sectors Disk Size), 32 Outstanding I/Os (QD=32), Full Random Data pattern, 4KB Align I/Os and test time duration was 15 minutes.

3.3 Latency

Table 3-3: Latency

Capacity / Latency	8 GB	16 GB	32 GB	64 GB
4K Read latency (ms)	0.09	0.07	0.06	0.06
4K Write latency (ms)	0.27	0.11	0.06	0.05

Note:
1. Results may differ from various flash configurations or host system settings.
2. Latencies are measured by IOMeter on full LBA, 1 Outstanding I/Os (QD=1), Seq. Read/Write, Full Random Data pattern, 4KB Align I/Os and test time 5mins
3. Test environment: Intel Core i5 CPU, Chipset Intel® Z68, Windows 7 64-bit, and the tested device is used as storage.

3.4 Environmental Specifications

Table 3-4 Environmental specifications

Item	Specification
Operating temperature (standard)	0~70℃
Operating temperature (extended)	-40℃ ~ +85℃
Storage temperature	-40℃ ~ +85℃
Humidity	Operating: 40℃, 90% RH Storage: 40℃, 93% RH
ESD (Electrostatic Discharge)*	23℃, 49% (RH)
Acoustic	0dB

*Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.5 Certification and Compliance

- CE
- FCC
- RoHS
- BSMI

4. Flash Management

4.1 Error Correction/Detection

The ECC engine in this device can detect and correct up to 72 bits error in 1K bytes.

4.2 Flash Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Thus, this device implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

4.3 Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media. Apacer provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

4.4 Power Failure Management

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, the uSDC applies the flushing mechanism which requests the controller to transfer data to the cache. For this uSDC, SDR performs as a cache, and its sizes include 8MB or 32MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, the uSDC applies an algorithm to reduce the amount of data resides in the cache to provide a better performance by allowing incoming data to only have a “pit stop” in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (random 4K), the cache will be treated as an “organizer”, consolidating incoming data into groups before written into the flash to improve write amplification.

In sum, with this power failure management, uSDC proves to provide the reliability required by consumer, industrial, and enterprise-level application.

4.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

4.6 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

4.7 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

4.8 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 µs (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- DEVSLP (Device Sleep): triggered by interface signal, PHY might be powered down, the device in a almost shut down state, consuming less power than Slumber mode, host support required for this mode

Note: the behaviors of power management features would depend on host/device settings.

5. Software Interface

5.1 Command Set

Code	Command	Code	Command
00h	NOP	97h	Idle
06h	Data Set Management	98h	Check Power Mode
10h-1Fh	Recalibrate	99h	Sleep
20h	Read Sectors	B0h	SMART
21	Read Sectors without Retry	B1h	Device Configurations
24h	Read Sectors EXT	C4h	Read Multiple
25h	Read DMA EXT	C5h	Write Multiple
27h	Read Native Max Address EXT	C6h	Set Multiple Mode
29h	Read Multiple EXT	C8h	Read DMA
2Fh	Read Log EXT	C9h	Read DMA without Retry
30h	Write Sectors	CAh	Write DMA
31h	Write Sectors without Retry	CBh	Write DMA without Retry
34h	Write Sectors EXT	CEh	Write Multiple FUA EXT
35h	Write DMA EXT	E0h	Standby Immediate
37h	Set Native Max Address EXT	E1h	Idle Immediate
38h	CFA Write Sectors without Erase	E2h	Standby
39h	Write Multiple EXT	E3h	Idle
3Dh	Write DMA FUA EXT	E4h	Read Buffer
3Fh	Write Long EXT	E5h	Check Power Mode
40h	Read Verify Sectors	E6h	Sleep
41h	Read Verify Sectors without Retry	E7h	Flush Cache
42h	Read Verify Sectors EXT	E8h	Write Buffer
45h	Write Uncorrectable EXT	EAh	Flush Cache EXT
60h	Read FPDMA Queued	ECh	Identify Device
61h	Write FPDMA Queued	EFh	Set Features
70h-7Fh	Seek	F1h	Security Set Password
90h	Execute Device Diagnostic	F2h	Security Unlock
91h	Initialize Device Parameters	F3h	Security Erase Prepare
92h	Download Microcode	F4h	Security Erase Unit
93h	Download Microcode DMA	F5h	Security Freeze Lock
94h	Standby Immediate	F6h	Security Disable Password
95h	Idle Immediate	F8h	Read Native Max Address
96h	Standby	F9h	Set Max Address

6. Electrical Specification

Table 6-1: Operating Voltage

Parameter	Voltage	Range
VCC	3.3V	3.135V ~ 3.465V
VCCQ	1.8V	1.71V ~ 1.89V
VDDC	1.2V	1.14V ~ 1.26V
VDD	1.2V	1.14V ~ 1.26V

Table 6-2: Power consumption based on 3.3V (typical)

Capacity / Modes	8 GB	16 GB	32 GB	64 GB
Active (mA)	270	320	445	445
Idle (mA)	90	90	90	90

Note: Results may differ from various flash configurations or platforms.

6.1 uSDC Power Current & Circuit

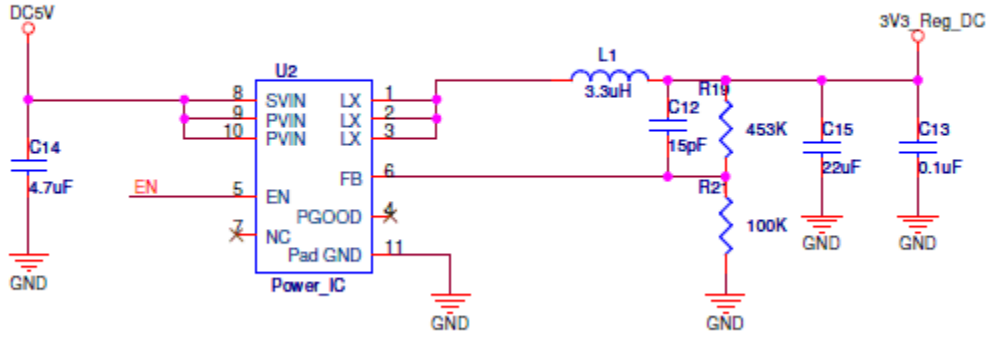
Since the uSDC operates on 3 levels of voltage requirements: 3.3V, 1.8V and 1.2V, the power current measurements were conducted respectively.

Typical Power Consumption

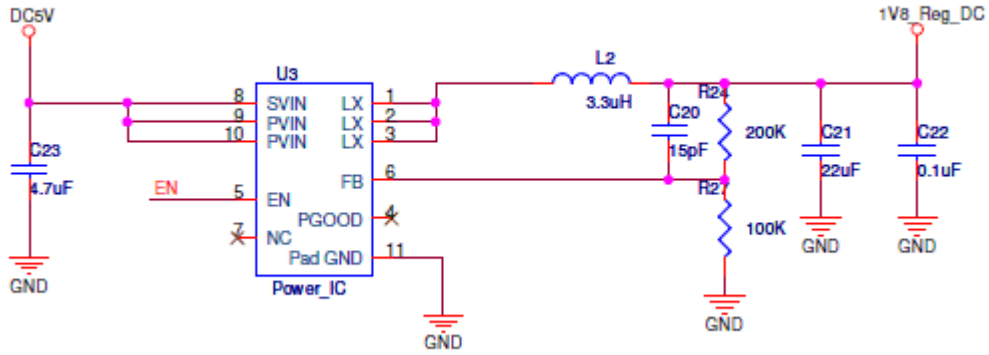
8GB	3.3v	1.8v	1.2v	16GB	3.3v	1.8v	1.2v
Power-on	100 mA	80 mA	300 mA	**Power-on**	100 mA	80 mA	300 mA
Idle	35 mA	100 uA	150 mA	**Idle**	35 mA	100 uA	150 mA
Active	100 mA	80 mA	350 mA	**Active**	140 mA	100 mA	380 mA
32GB	**3.3v**	**1.8v**	**1.2v**	**64GB**	**3.3v**	**1.8v**	**1.2v**
Power-on	100 mA	80 mA	300 mA	**Power-on**	100 mA	150 mA	300 mA
Idle	35 mA	150 uA	150 mA	**Idle**	35 mA	400 uA	150 mA
Active	220 mA	130 mA	460 mA	**Active**	220 mA	170 mA	460 mA

Notes: The results of “typical” power consumption were based on the maximum value measured from the experiment.

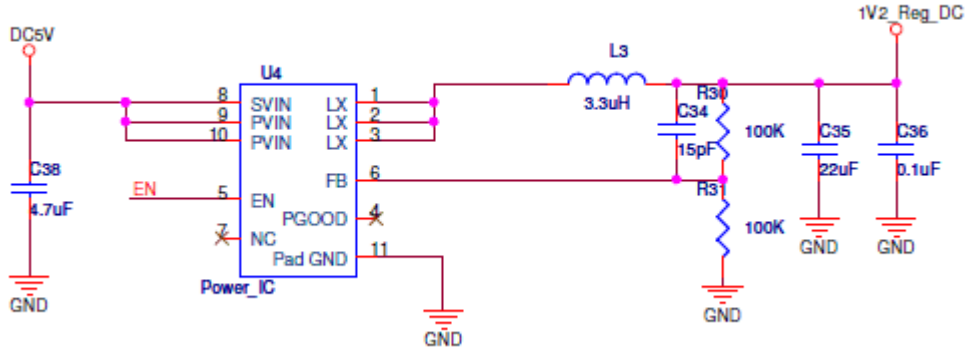
+3V3 Circuit



+1V8 Circuit

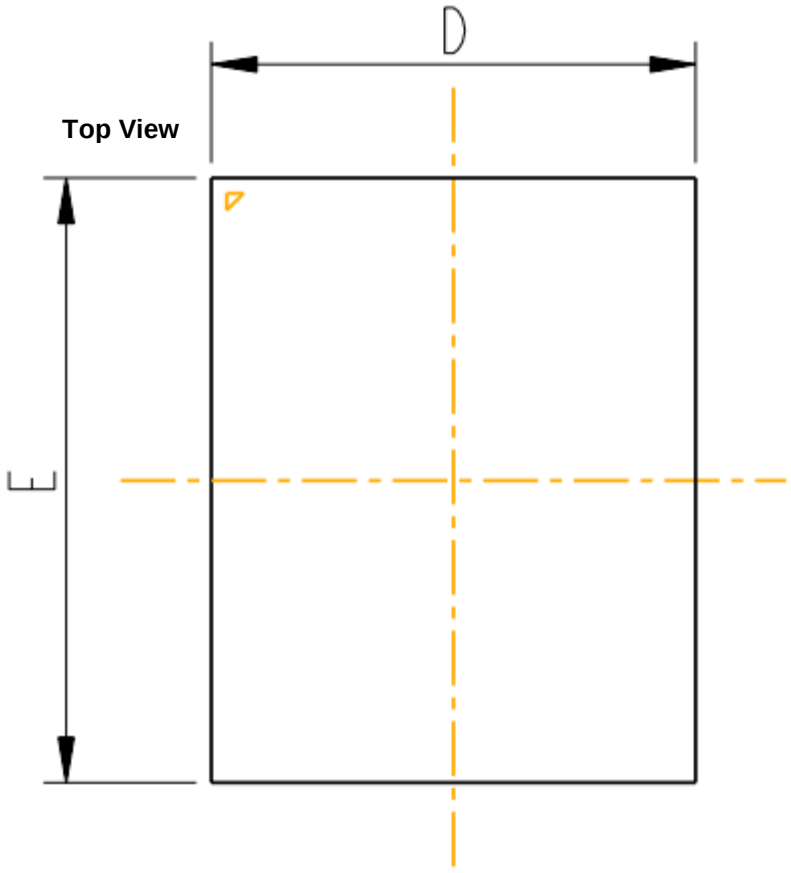


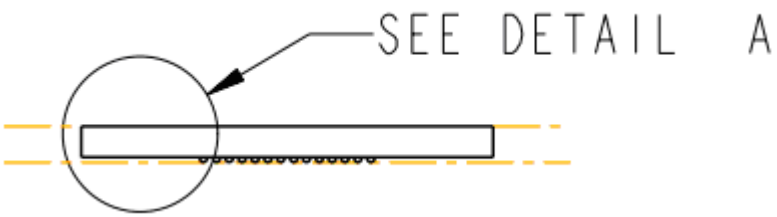
+1V2 Circuit



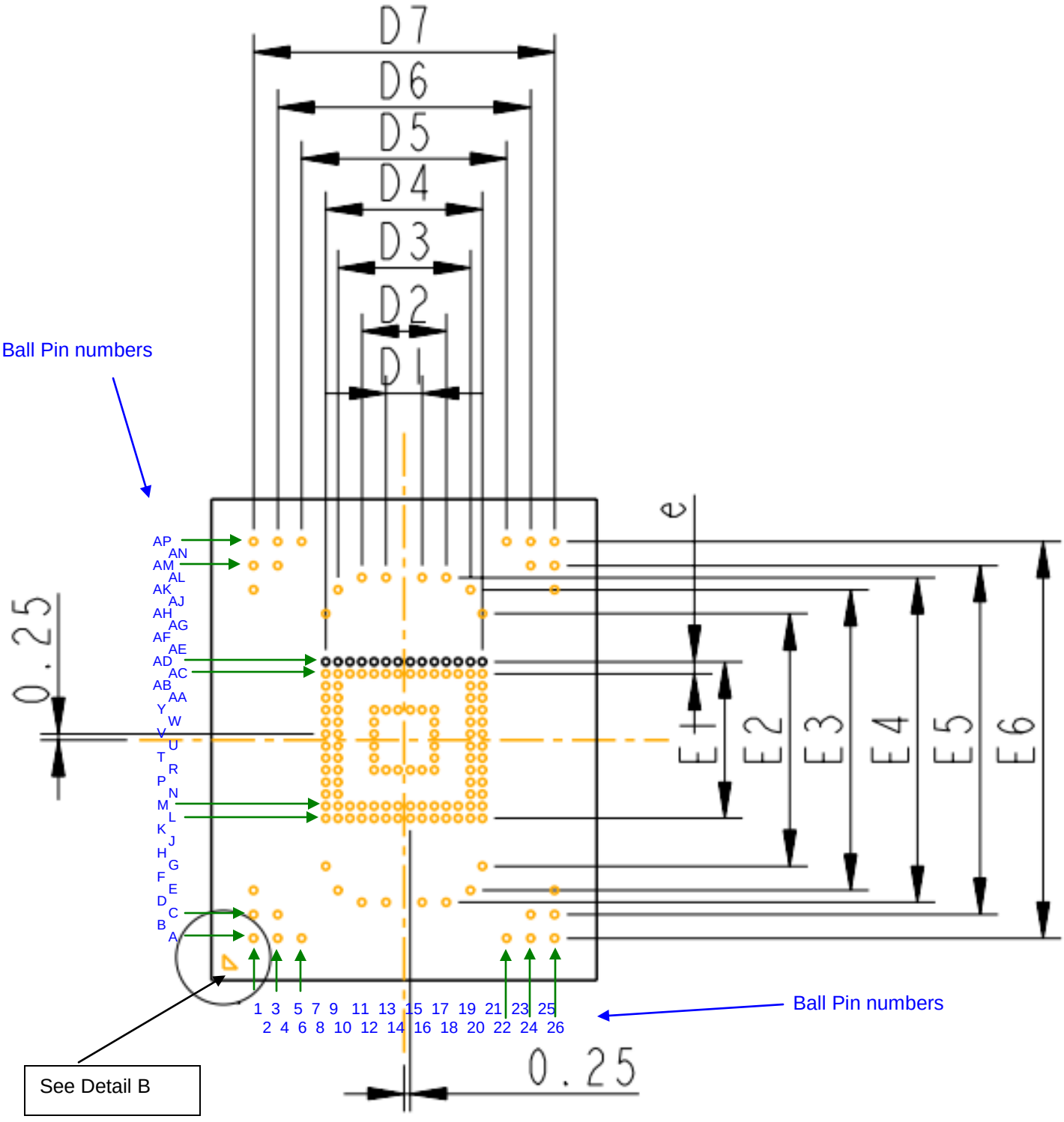
Notes: the Power IC used in the diagrams above is able to deliver up to 3A output current in case of changes or replacement in NAND Flash memories.

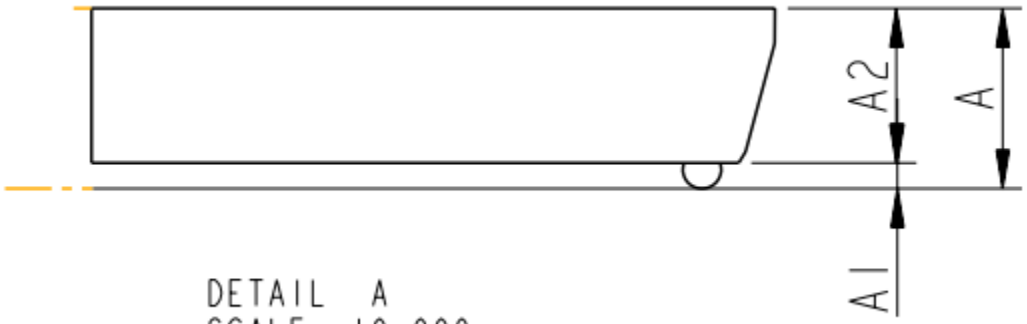
7. Mechanical Specifications



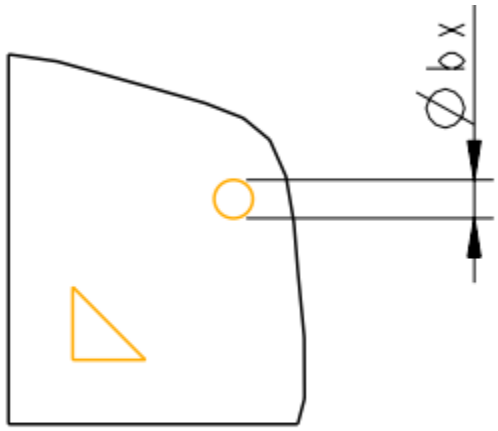


Bottom View





DETAIL A
SCALE 10.000



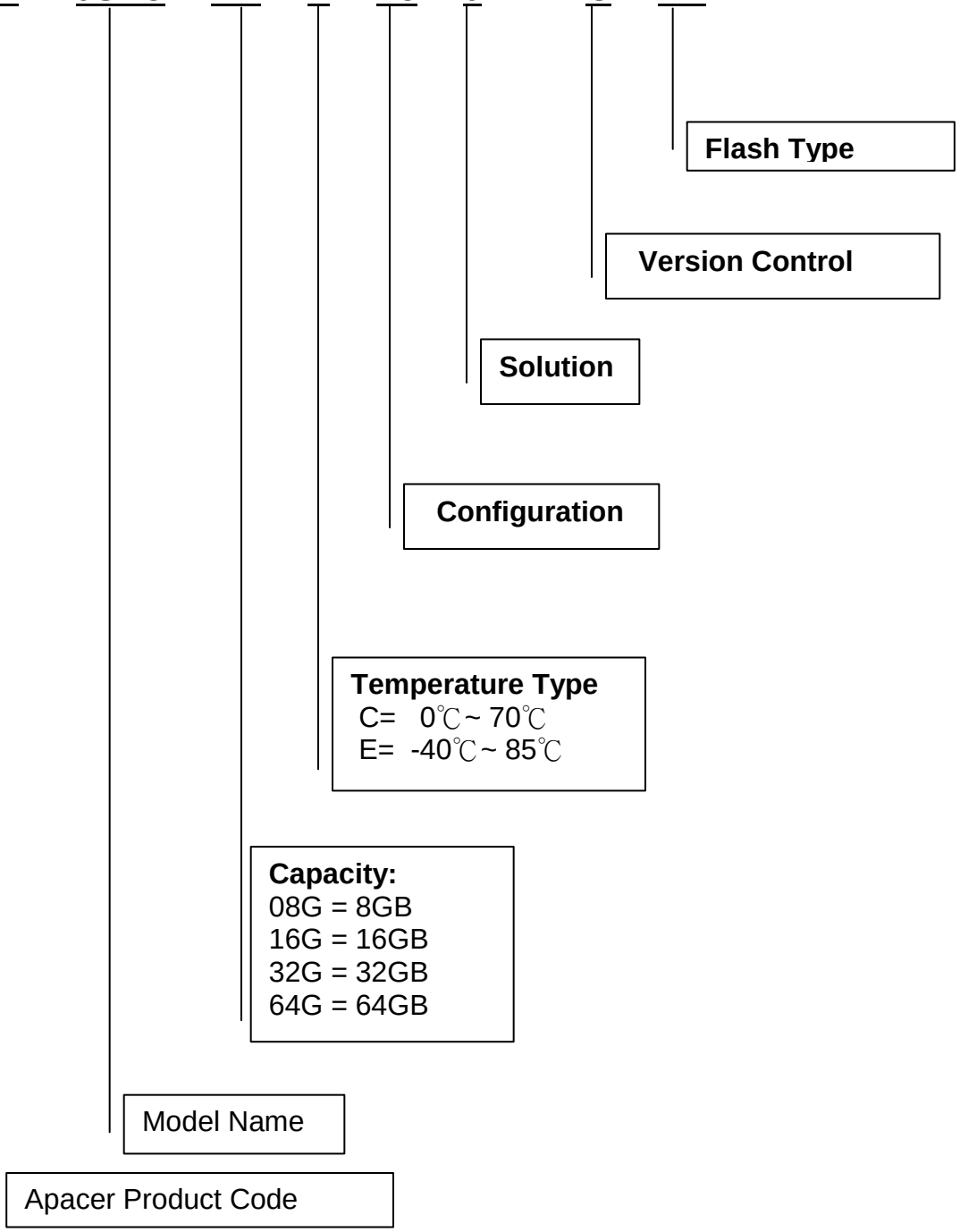
DETAIL B
SCALE 10.000

Symbol	Dimension		
	MIN	NOM	MAX
A	---	---	1.40
A1	0.15	---	---
A2	---	---	1.20
D	15.85	16	16.15
E	19.85	20	20.15
D1	---	1.5	---
D2	---	3.5	---
D3	---	5.5	---
D4	---	6.5	---
D5	---	8.5	---
D6	---	10.5	---
D7	---	12.5	---
E1	---	6.5	---
E2	---	10.5	---
E3	---	12.5	---
E4	---	13.5	---
E5	---	14.5	---
E6	---	16.5	---
e	---	0.50	---
b	0.25	0.30	0.35

8. Product Ordering Information

8.1 Product Code Designation

A P - uSDC xxx X X3 9 - G TM



8.2 Valid Combination

8.2.1 Standard Temperature (0℃ ~ 70℃)

Capacity	Part Number	Top Side Marking
8GB	AP-USDC08GC139-GTM	SH9B-8GCCA11HA
16GB	AP-USDC16GC239-GTM	SH9B-16GCCA22HA
32GB	AP-USDC32GC439-GTM	SH9B-32GCCA44HA
64GB	AP-USDC64GC839-GTM	SH9B-64GCCB48HA

8.2.2 Extended Temperature (-40℃ ~ 85℃)

Capacity	Part Number	Top Side Marking
8GB	AP-USDC08GE139-GTM	SH9B-8GCEA11HA
16GB	AP-USDC16GE239-GTM	SH9B-16GCEA22HA
32GB	AP-USDC32GE439-GTM	SH9B-32GCEA44HA
64GB	AP-USDC64GE839-GTM	SH9B-64GCEB48HA

Note: Please consult with Apacer sales representatives for availabilities.

Revision History

Revision	Date	Description	Remark
1.0	11/01/2013	Official release	
1.1	12/18/2013	Updated mechanical drawing Removed Device Sleep	
1.2	01/27/2014	Added Device Sleep back into the document due to firmware upgrade	
1.3	03/12/2014	Revised performance and power consumption due to firmware version update	
1.4	05/20/2014	Upgraded temperature specification: from “Enhanced” (-25℃ to 85℃) to “Extended” grade (-40℃ to 85℃)	
1.5	07/10/2014	Added uSDC power circuit and current section	
1.6	08/04/2014	Enlarged the mechanical drawings and pin assignment illustrations Add ball pin numbers on the bottom view of the mechanical drawing Added green arrows indicating pin locations	
1.7	08/08/2014	Added top side marking in product ordering information	
1.8	09/02/2014	Simplified description for Device Sleep in Pin Assignment section	
1.9	06/08/2015	Revised product ordering information due to flash and firmware change	
2.0	06/17/2015	Updated pin definition : L15(XTRST), L16(XTDI), L17(XTDO), L18(XTCK), AA8(XTMS), AD7(XTM0) are for Apacer internal debug use.	

Global Presence

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