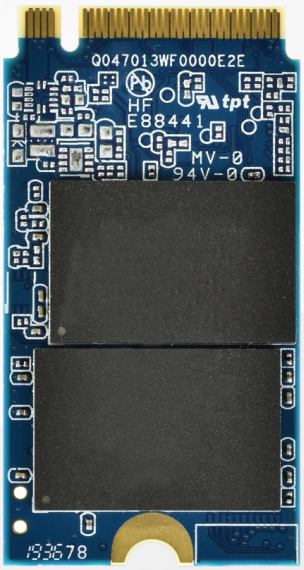
Apacer

RoHS Compliant

PCI Express Flash Drive

Industrial PT15R-M242 BiCS5 Product Specifications



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Specifications Overview:

- **PCIe Interface**
  - Compliant with PCI Express 3.1
  - Compliant with NVMe 1.3
  - Compatible with PCIe Gen3 x4 interface
- **Capacity**
  - 64, 128, 256, 512 GB
- **Performance**[1]
  - Interface burst read/write: 4 GB/sec
  - Sequential read: up to 2,445 MB/sec
  - Sequential write: up to 1,750 MB/sec
  - Random read (4K): up to 235,000 IOPS
  - Random write (4K): up to 399,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash Bad-Block Management
  - Flash Translation Layer: Page Mapping
  - Power Failure Management
  - S.M.A.R.T.
  - TRIM
  - Hyper Cache Technology
  - DataRAID™
  - NVMe Secure Erase
- **NVMe Features**[2]
  - Supports HMB (Host Memory Buffer)
- **NAND Flash Type:** 3D TLC (BiCS5)
- **MTBF:** >2,000,000 hours
- **Endurance (in drive writes per day: DWPD)**
  - 64 GB: 1.54 DWPD
  - 128 GB: 1.1 DWPD
  - 256 GB: 1 DWPD
  - 512 GB: 1.05 DWPD
- **Temperature Range**
  - Operating (Tc): 0°C to 70°C
  - Storage (Ta): -40°C to 85°C
- **Supply Voltage**
  - 3.3V ± 5%
- **Power Consumption**[1]
  - Active mode (Max.): 905 mA
  - Idle mode: 180 mA
- **Power Management**
  - Supports APST
  - Supports ASPM L1.2
- **Reliability**
  - Thermal Sensor
  - Thermal Throttling
  - End-to-End Data Protection
- **Connector Type**
  - 75-pin M.2 module pinout
- **Physical Characteristics**
  - Form factor: Double-sided M.2 2242-D2-M
  - Dimensions: 42.00 x 22.00 x 3.58(max.), unit: mm
  - Net weight: 4.61g ± 5%
- **RoHS Compliant**

Notes:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.
2. Windows 10 (version 1703) onwards supports the HMB (Host Memory Buffer) function.

Table of Contents

1. General Description

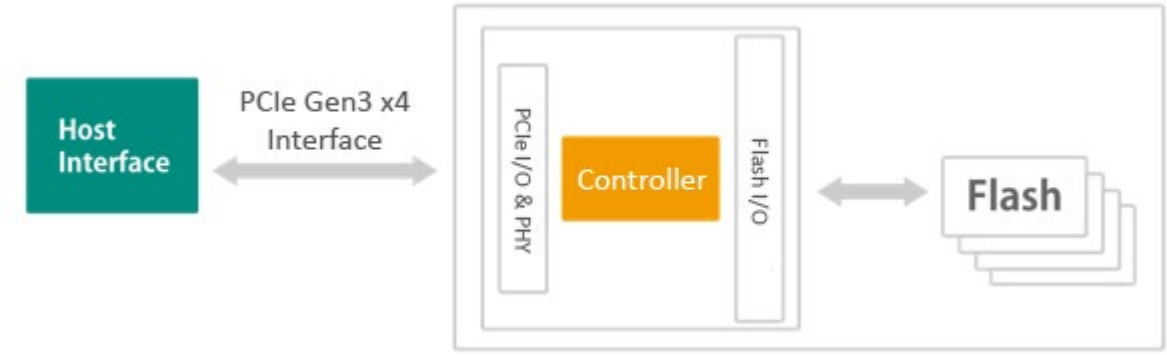
Apacer PT15R-M242 is the fastest SSD designed with M.2 2242 mechanical dimensions, fully compliant with the PCIe Gen3 x4 interface and NVMe 1.3 specifications. This compliance enables it to operate in power management modes, significantly reducing power consumption. Equipped with a powerful PCIe controller that supports on-the-module ECC and an efficient wear-leveling scheme, PT15R-M242 delivers exceptionally low latency and outstanding data transfer performance. Its compact, high-speed storage makes it the ideal choice for larger, faster hosts in a wide range of applications requiring superior performance.

Leveraging 3D NAND technology for capacities of up to 512GB and offering greater power efficiency than 2D NAND, PT15R-M242 integrates an LDPC (Low-Density Parity Check) ECC engine to enhance SSD endurance and data reliability. It also features a built-in thermal sensor to monitor SSD temperatures via S.M.A.R.T commands, complemented by thermal throttling that dynamically adjusts frequency scaling to ensure sustained performance and prevent overheating. For highly intensive applications, End-to-End Data Protection ensures data integrity at multiple points along the data transfer path, ensuring reliable delivery.

In terms of flash management, PT15R-M242 incorporates various advanced features, including flash block management, page mapping, TRIM, power failure management, Hyper Cache technology, DataRAID, NVMe secure erase, and power-saving modes.

With exceptional performance and enhanced reliability, PT15R-M242 is the ideal storage or cache solution for a variety of applications, including industrial, imaging, computing, and enterprise markets.

2. Functional Block



Note: The actual number of NAND flash used on Apacer PT15R-M242 varies from capacities. The illustration is for reference only.

Figure 2-1 Functional Block Diagram

3. Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into Key M connectors.

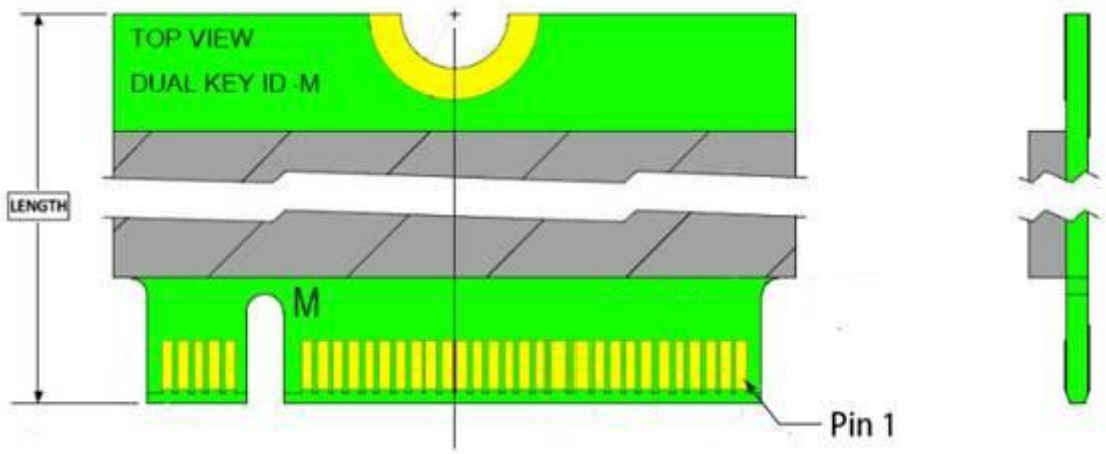


Figure 3-1 Pin Connectors

Table 3-1 Pin Assignments

Pin No.	Type	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect[1]
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec

Table 3-1 Pin Assignments

Pin No.	Type	Description
20	N/C	No connect[1]
21	GND	Ground
22	N/C	No connect[1]
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect[1]
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect[1]
27	GND	Ground
28	N/C	No connect[1]
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect[1]
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect[1]
33	GND	Ground
34	N/C	No connect[1]
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect[1]
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect[1]
39	GND	Ground
40	N/C	No connect[1]
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	N/C	No connect[1]
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	N/C	No connect[1]
45	GND	Ground
46	N/C	No connect[1]
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect[1]
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	N/C	No connect[1]
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground

Table 3-1 Pin Assignments

Pin No.	Type	Description
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	Module Key
61	Module Key M	Module Key
62	Module Key M	Module Key
63	Module Key M	Module Key
64	Module Key M	Module Key
65	Module Key M	Module Key
66	Module Key M	Module Key
67	N/C	No connect[1]
68	N/C	No connect[1]
69	N/C	No connect[1]
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	CONFIG_2 = Ground

Note:
1. Reserved by Apacer, please do not connect to a host.

4. Product Specifications

4.1 Capacity

Capacity specifications of PT15R-M242 are available as shown in Table 4-1.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Total LBA
64 GB	64,023,257,088	125,045,424
128 GB	128,035,676,160	250,069,680
256 GB	256,060,514,304	500,118,192
512 GB	512,110,190,592	1,000,215,216

Notes:
- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PT15R-M242 is listed below in Table 4-2.

Table 4-2 Performance Specifications

Performance \ Capacity	64 GB	128 GB	256 GB	512 GB
Sequential Read (MB/s)	570	1,145	2,310	2,445
Sequential Write (MB/s)	415	555	1,110	1,750
4K Random Read (IOPS)	47,000	96,000	164,000	235,000
4K Random Write (IOPS)	84,000	124,000	249,000	399,000

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 128.

4.3 Environmental Specifications

Environmental specifications of PT15R-M242 are shown in Table 4-3.

Table 4-3 Environmental Specifications

Environment	Type		Specifications
Temperature	Operating (Tc)		0°C to 70°C
	Non-operating (Ta)		-40°C to 85°C
Vibration	Non-operating	Frequency/Displacement	20Hz~80Hz/1.52mm
		Frequency/Acceleration	80Hz~2000Hz/20G
Shock	Non-operating		1,500(G), half-sine wave

Notes:

- This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.
- Tc: case temperature; Ta: ambient temperature. The operating temperature is determined by the case temperature. Adequate airflow is advisable as it enables the device to maintain optimal temperatures, especially in environments with heavy workloads.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PT15R-M242. The prediction result for PT15R-M242 is more than 2,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PT15R-M242 complies with the following standards:

- CE
- UKCA
- FCC
- RoHS

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	Drive Writes Per Day
64 GB	1.54
128 GB	1.1
256 GB	1
512 GB	1.05

Notes:

- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycles: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 3 years)

5. Flash Management

5.1 Error Correction/Detection

PT15R-M242 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.6 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.7 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.8 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

5.9 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

6. NVMe Support Features

6.1 Host Memory Buffer

Host Memory Buffer (HMB) allows HOST to allocate system memory for SSD's exclusive use in order to provide better performance and endurance, especially for DRAMless solutions.

7. Reliability Features

7.1 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

7.2 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

7.3 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

8. Software Interface

8.1 Command Set

Table 8-1 summarizes the commands supported by PT15R-M242.

Table 8-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test
18h	Keep Alive

Table 8-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM

Table 8-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
08h	Write Zeroes
09h	Dataset Management

8.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 8-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1
202-203	2	Temperature Sensor 2
204-205	2	Temperature Sensor 3
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8
216-511	296	Reserved

Note: Temperature display of the Temperature Sensor from 1 to 8 (corresponding bytes from 200 to 215) is not supported if the return value is 0h.

Table 8-5 SMART (C0h)

Byte	Length	Description
0-255	256	Reserved
256-257	2	SSD Protect Mode
258-261	4	Host Read UNC Count
262-265	4	PHY Error Count
266-269	4	Reserved
270-273	4	Total Early Bad Block Count
274-277	4	Total Later Bad Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	Flash Write Sector
302-305	4	Total Spare Block
306-309	4	Current Spare Block
310-313	4	Read Retry Count
314-511	210	Reserved

9. Electrical Specifications

9.1 Operating Voltage

Table 9-1 lists the supply voltage for PT15R-M242.

Table 9-1 Operating Range

Item	Range
Supply Voltage	3.3V ± 5%

9.2 Power Consumption

Table 9-2 lists the power consumption for PT15R-M242.

Table 9-2 Power Consumption

Capacity / Mode	Unit	64 GB	128 GB	256 GB	512 GB
Active (Max.)	mA	415	560	840	905
Idle		185	180	180	180

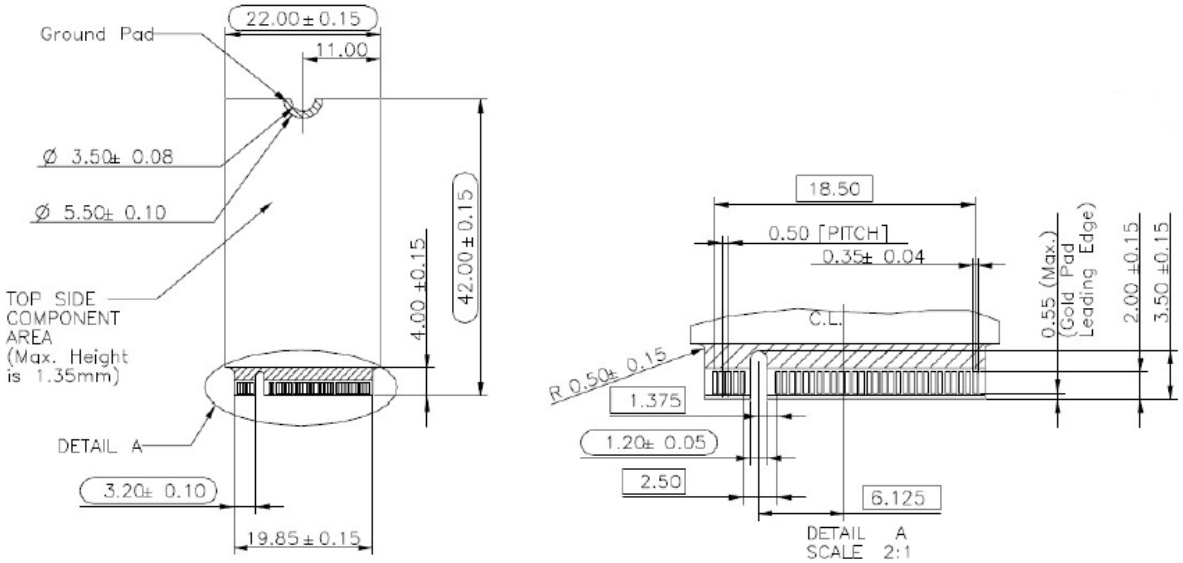
Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 8.0.4 with file size 1,000MB.

10. Mechanical Specifications

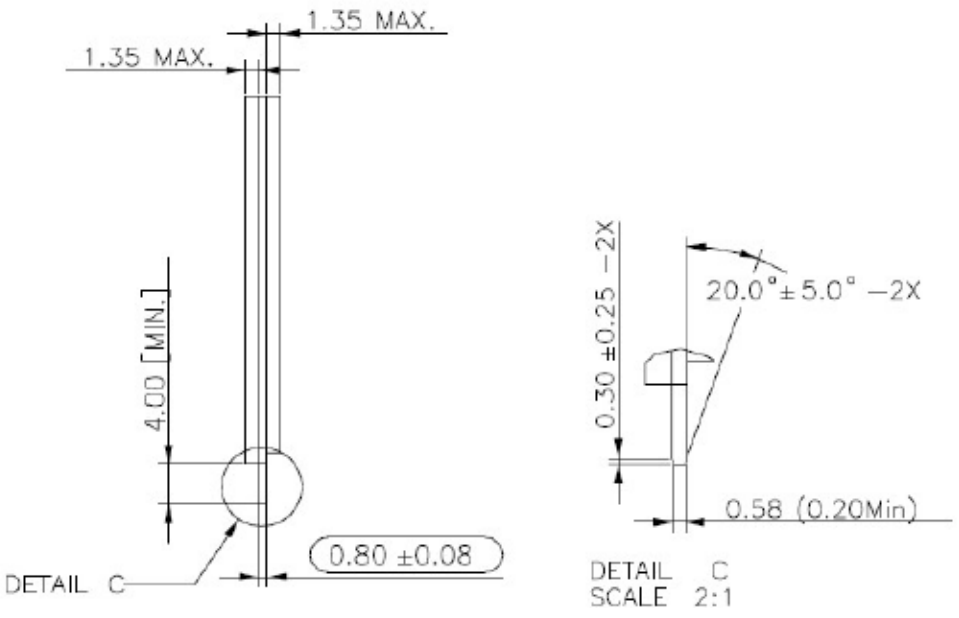
Table 10-1 Physical Information

Parameter	Unit	64 GB	128 GB	256 GB	512 GB
Length	mm	42.00 ± 0.15			
Width		22.00 ± 0.15			
Height (Max.)		3.58			
Weight	g ± 5%	3.3	3.57	3.73	4.61

Top View



Side View



Bottom View

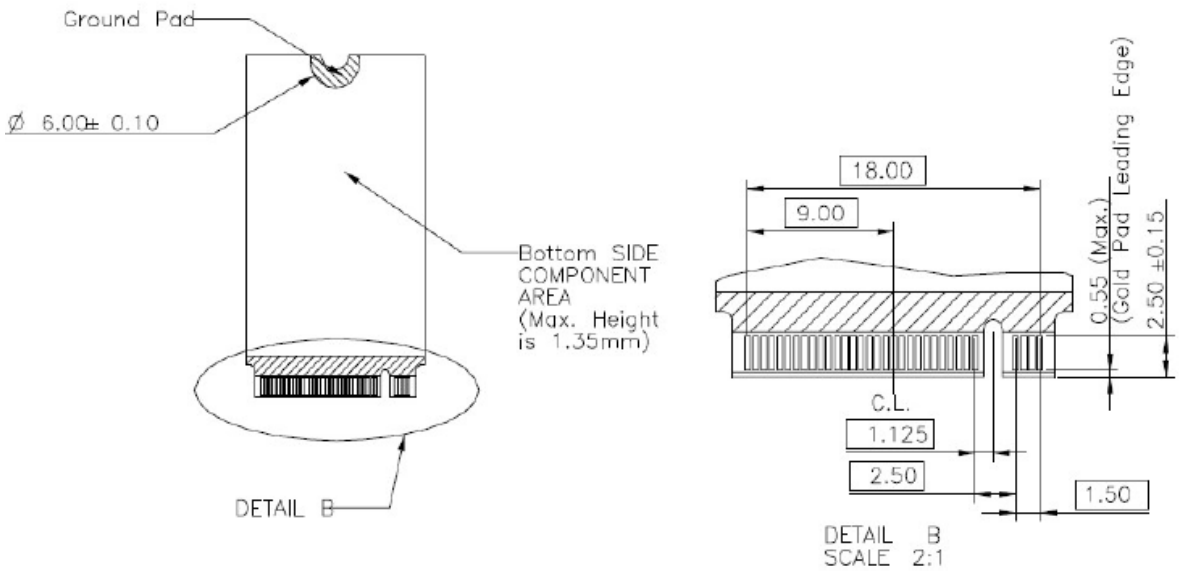


Figure 10-1 Physical Dimensions

Notes :
1. = Max Component Height
2. = No Component
3. = No Component / Signal Vias / Signal Copper / Printing
4. General Tolerance ±0.15mm
5. are critical dimensions

11. Product Ordering Information

11.1 Product Code Designations

Apacer's PT15R-M242 SSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the PT15R-M242 series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	7	6	.	1	5	2	X	G	D	.	X	X	X	X	X

Code 1-3 (Product Line & Form Factor)	PCIe
Code 5-6 (Model/Solution)	PT15R-M242
Code 7-8 (Product Capacity)	2G: 64GB 2H: 128GB 2J: 256GB 2K: 512GB
Code 9 (Flash Type & Product Temp)	3D TLC Standard Temperature
Code 10 (Product Spec)	Double-sided M key
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	10: 64GB 03: 128/256/512GB

11.2 Valid Combinations

The following table lists the available models of the PT15R-M242 series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Valid Combination
64GB	B76.152GGD.00110
128GB	B76.152HGD.00203
256GB	B76.152JGD.00203
512GB	B76.152KGD.00103

Revision History

Revision	Description	Date
1.0	Initial release	11/27/2024
1.1	Changed model name from PT150-M242 to PT15R-M242	12/31/2024

Global Presence

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