RoHS Compliant

16GB REGISTERED DDR5 SDRAM DIMM

Halogen free

Product Specifications

May 9, 2022

Version 1.0

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General Description

Apacer **D52.31282S.001** is a 16GB DDR5 SDRAM (Synchronous DRAM) ECC Registered DIMM. This memory module consists of 10 pieces 2G x 8 bits DDR5 synchronous DRAMs in FBGA packages and 8K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Density	Speed	Organization	DRAM Composition	Rank
D52.31282S.001	16GB	4800 Mbps	2Gx80	2Gx8 *10	1

Key Parameters

Speed	DDR5-4800	Unit
	-CL40	
tCK (min)	0.416	ns
CAS latency	40	nCK
tRCD (min)	16	ns
tRP (min)	16	ns
tRAS (min)	32	ns
tRC (min)	48	ns
CL-tRCD-tRP	40-39-39	nCK

Features:

- JEDEC standard compliant
- Support ECC error detection and correction
- On-DIMM thermal sensor : Yes
- PCB: height 31.25 mm, lead pitch 0.85 mm (pin),
- VDD = VDDQ= 1.1V (1.067V to 1.166V)
- VPP = 1.8V (1.746V to 1.908V)、VDDSPD = 1.8V
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- CAS Latency (CL): 22,26,28,30,32,36,40,42
- CAS Write Latency (CWL): RL-2
- Operating temperature Tcase–(0℃~85℃)
- Average Refresh period 3.9us at lower than Tcase 85°C, 1.95us at 85°C < Tcase < 95 °C.
- All bank and same bank refresh
- Bi-Directional Differential Data Strobe
- 16-bit prefetch architecture
- On-die ECC
- ECC transparency and error scrub
- sPPR and hPPR capability
- Halogen free、Lead-free (RoHS compliant)
- PCB: 30μ inch gold finger

Pin Assignments

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
1	VIN_BULK	145	VIN_BULK	74	PAR_A	218	CK_c
2	RFU	146	VIN_BULK	75	VSS	219	VSS
3	VIN_MGMT	147	PWR_GOOD /FAIL_n	76	CA0_B	220	RFU
4	SCL	148	SAA	77	VSS	221	CA1_B
5	SDA	149	RFU	78	CA2_B	222	VSS
6	VSS	150	RFU	79	VSS	223	CA3_B
7	DQ0_A	151	VSS	80	CA4_B	224	VSS
8	VSS	152	DQ2_A	81	VSS	225	CA5_B
9	DQ1_A	153	VSS	82	CA6_B	226	VSS
10	VSS	154	DQ3_A	83	VSS	227	PAR_B
11	DQS0_A_t	155	VSS	84	CS0_B_n	228	VSS
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	85	VSS	229	CS1_B_n
13	VSS	157	DQS5_A_t, TDQS5_A_t	86	LBD,RSP_A_n	230	VSS
14	DQ4_A	158	VSS	87	LBS,RSP_B_n	231	RFU
15	VSS	159	DQ6_A	88	VSS	232	RFU
16	DQ5_A	160	VSS	89	CB4_B	233	VSS
17	VSS	161	DQ7_A	90	VSS	234	CB6_B
18	DQ8_A	162	VSS	91	CB5_B	235	VSS
19	VSS	163	DQ10_A	92	VSS	236	CB7_B
20	DQ9_A	164	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS
21	VSS	165	DQ11_A	94	DQS9_B_c, TDQS9_B_c	238	DQS4_B_c
22	DQS1_A_t	166	VSS	95	VSS	239	DQS4_B_t
23	DQS1_A_c	167	DQS6_A_c, TDQS6_A_c	96	CB0_B	240	VSS
24	VSS	168	DQS6_A_t, TDQS6_A_t	97	VSS	241	CB2_B
25	DQ12_A	169	VSS	98	CB1_B	242	VSS
26	VSS	170	DQ14_A	99	VSS	243	CB3_B
27	DQ13_A	171	VSS	100	DQ0_B	244	VSS
28	VSS	172	DQ15_A	101	VSS	245	DQ2_B
29	DQ16_A	173	VSS	102	DQ1_B	246	VSS
30	VSS	174	DQ18_A	103	VSS	247	DQ3_B
31	DQ17_A	175	VSS	104	DQS0_B_t	248	VSS
32	VSS	176	DQ19_A	105	DQS0_B_c	249	DQS5_B_c,TDQS5_B_c
33	DQS2_A_t	177	VSS	106	VSS	250	DQS5_B_t, TDQS5_B_t
34	DQS2_A_c	178	DQS7_A_c, TDQS7_A_c	107	DQ4_B	251	VSS
35	VSS	179	DQS7_A_t, TDQS7_A_t	108	VSS	252	DQ6_B
36	DQ20_A	180	VSS	109	DQ5_B	253	VSS
37	VSS	181	DQ22_A	110	VSS	254	DQ7_B
38	DQ21_A	182	VSS	111	DQ8_B	255	VSS
39	VSS	183	DQ23_A	112	VSS	256	DQ10_B

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
40	DQ24_A	184	VSS	113	DQ9_B	257	VSS
41	VSS	185	DQ26_A	114	VSS	258	DQ11_B
42	DQ25_A	186	VSS	115	DQS1_B_t	259	VSS
43	VSS	187	DQ27_A	116	DQS1_B_c	260	DQS6_B_c, TDQS6_B_c
44	DQS3_A_t	188	VSS	117	VSS	261	DQS6_B_t, TDQS6_B_t
45	DQS3_A_c	189	DQS8_A_c, TDQS8_A_c	118	DQ12_B	262	VSS
46	VSS	190	DQS8_A_t, TDQS8_A_t	119	VSS	263	DQ14_B
47	DQ28_A	191	VSS	120	DQ13_B	264	VSS
48	VSS	192	DQ30_A	121	VSS	265	DQ15_B
49	DQ29_A	193	VSS	122	DQ16_B	266	VSS
50	VSS	194	DQ31_A	123	VSS	267	DQ18_B
51	CB0_A	195	VSS	124	DQ17_B	268	VSS
52	VSS	196	CB2_A	125	VSS	269	DQ19_B
53	CB1_A	197	VSS	126	DQS2_B_t	270	VSS
54	VSS	198	CB3_A	127	DQS2_B_c	271	DQS7_B_c, TDQS7_B_c
55	DQS4_A_t	199	VSS	128	VSS	272	DQS7_B_t, TDQS7_B_t
56	DQS4_A_c	200	DQS9_A_c, TDQS9_A_c	129	DQ20_B	273	VSS
57	VSS	201	DQS9_A_t, TDQS9_A_t	130	VSS	274	DQ22_B
58	CB4_A	202	VSS	131	DQ21_B	275	VSS
59	VSS	203	CB6_A	132	VSS	276	DQ23_B
60	CB5_A	204	VSS	133	DQ24_B	277	VSS
61	VSS	205	CB7_A	134	VSS	278	DQ26_B
62	ALERT_n	206	VSS	135	DQ25_B	279	VSS
63	VSS	207	RESET_n	136	VSS	280	DQ27_B
64	CS0_A_n	208	VSS	137	DQS3_B_t	281	VSS
65	VSS	209	CS1_A_n	138	DQS3_B_c	282	DQS8_B_c, TDQS8_B_c
66	CA0_A	210	VSS	139	VSS	283	DQS8_B_t, TDQS8_B_t
67	VSS	211	CA1_A	140	DQ28_B	284	VSS
68	CA2_A	212	VSS	141	VSS	285	DQ30_B
69	VSS	213	CA3_A	142	DQ29_B	286	VSS
70	CA4_A	214	VSS	143	VSS	287	DQ31_B
71	VSS	215	CA5_A	144	RFU	288	VSS
72	CA6_A	216	VSS				
73	VSS	217	CK_t				

Pin Descriptions

Pin Name	Description
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t	SDRAM Clocks (true/positive)
CK_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output

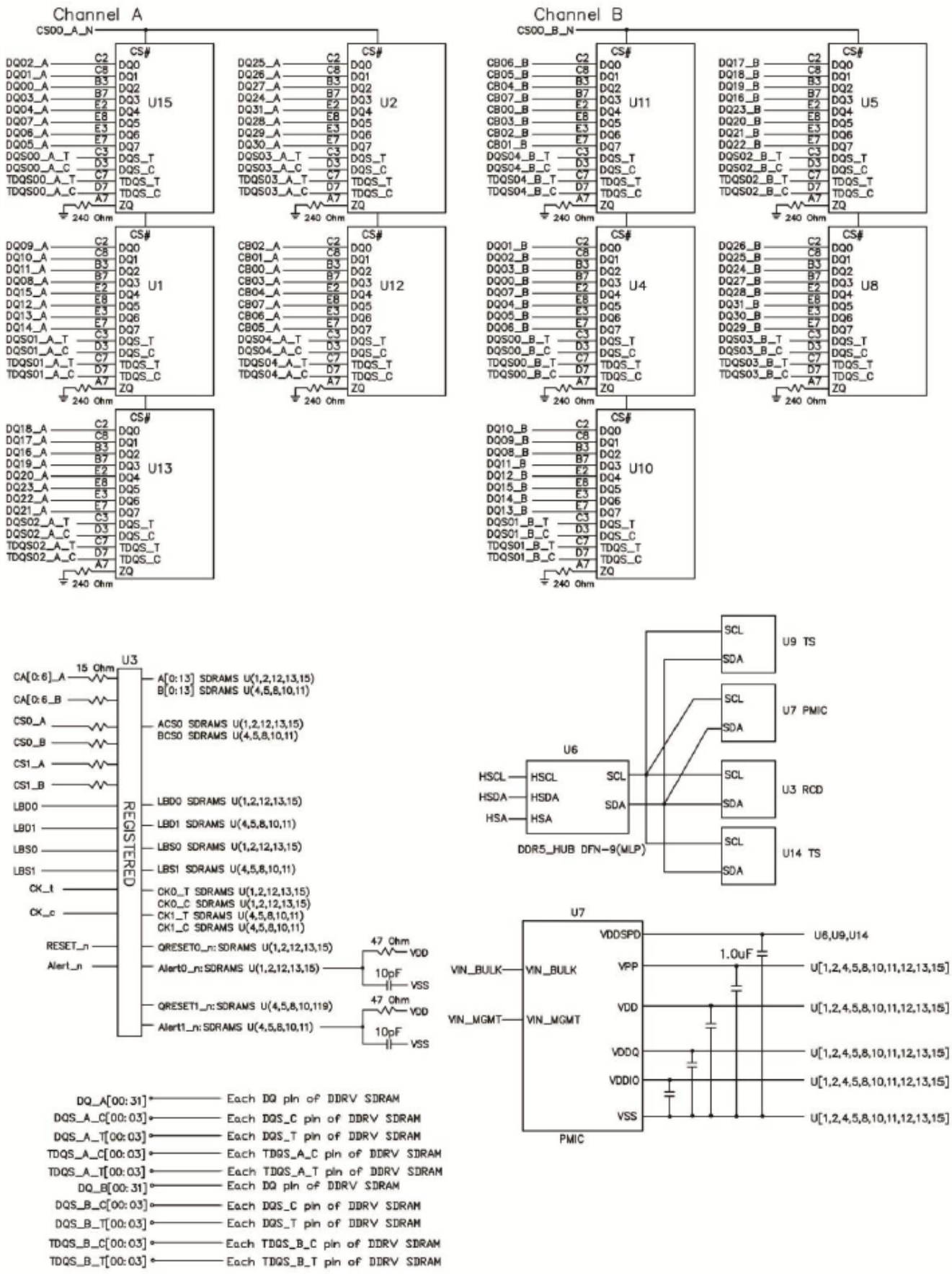
INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	I/O Levels	Description
CS[1:0]_A CS[1:0]_B	Input	VDD	Chip Select : All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR_A PAR_B	Input	VDD	Command and Address Parity Input: DDR5 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CSx_x_n LOW
ALERT_n	Output	VDD	Alert : If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system-dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Input Output	3.6V(max)	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).

Symbol	Type	I/O Levels	Description
HSCL	Input	VOUT_1.0 V	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	Input / Output	VOUT_1.0 V	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	Input	2.1V max	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation
DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	VDD	ECC Check Bits Input/ Output: Bi-directional data bus.
DQS[9:0]_A_t DQS[9:0]_B_t	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DQS[9:0]_A_c DQS[9:0]_B_c			
TDQS[9:5]_A_t TDQS[9:5]_B_t	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.
TDQS[9:5]_A_c TDQS[9:5]_B_c			

Symbol	Type	I/O Levels	Description
LBDQ	Output	VDDQ	Loopback data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled the pin is either terminated or Hi-Z based on MR36:OP[2:0].
LBDQS	Output	VDDQ	Loopback data strobe output: This is a single ended strobe with the rising edged aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36:OP[2:0].
RFU			Reserved for Future Use: No on DIMM electrical connection is present.
VIN_BULK	Supply		External power supply: 12V, 4.25V (min), 15V (max)
VIN_MGMT	Supply		External power supply: 3.3V, 3.0V (min), 3.6V (max)
VSS	Supply		Ground

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on VDD pin relative to Vss	V_{DD}	- 0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.3 ~ 1.4	V	1
Voltage on VPP pin relative to Vss	V_{PP}	- 0.3 ~ 2.1	V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.3 ~ 1.4	V	1
Storage temperature	TSTG	– 55 to +100	˚C	1,2

Notes:

1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

DRAM Component Operating Temperature Range

Symbol	Parameter	Temperature Range (Units : ℃)		Grade	Notes
		Min	Max		
Toper normal	Normal Operating Temperature	0	85	NT	1,2,3,4
Toper extended	Extended Operating Temperature	0	95	XT	1,2,3,4,5

Notes:

1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. All DDR5 SDRAMs are required to operate in NT and XT temperature ranges.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.

AC & DC OPERATING CONDITION

DIMM Voltage Requirements

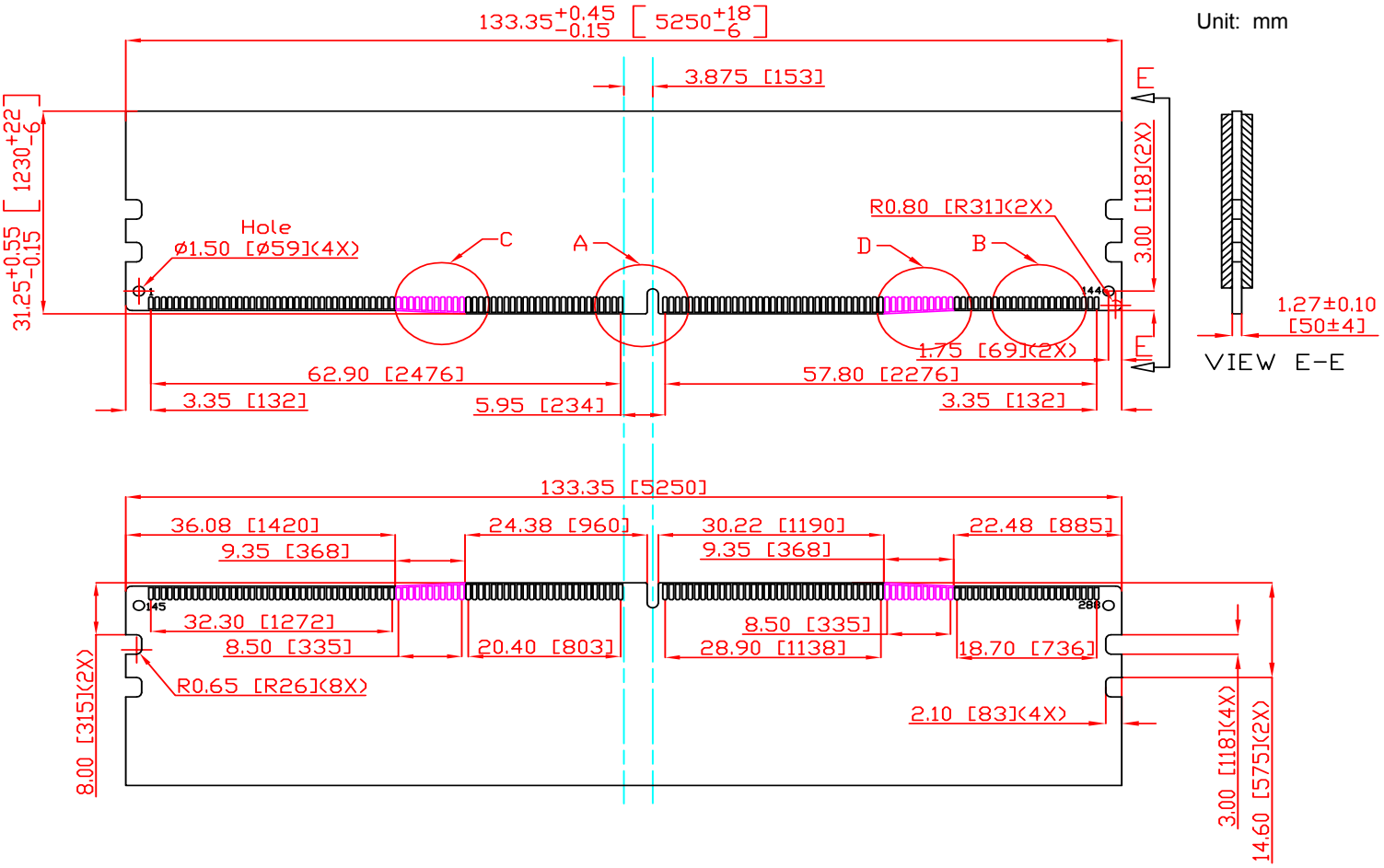
Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host Supply Voltage	4.25	12.0	15	2.5(maximum)	Operational
VIN_MGMT	Host Supply Voltage	3.0	3.3	3.6	0.110(minimum)	Operational
VDD	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
VDDQ	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
VPP	PMIC Output Supply Voltage	1.746	1.8	1.908	Note 5	Operational
1.8V LDO	PMIC Output Supply Voltage	Note 6	1.8	Note 6	0.025(maximum)	Operational
1.0V LDO	PMIC Output Supply Voltage	Note 6	1.0	Note 6	0.020(maximum)	Operational

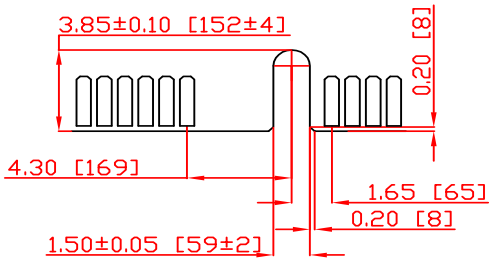
NOTE :

1. The SDRAM specification must be met and takes precedence over this document.
2. PMIC, Hub, TS, RCD specifications must be met and takes precedence over this document.
3. Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances.
4. Typical voltage is platform dependent. This is a suggested value only.
5. Maximum and Minimum Current ratings depend on PMIC (5000 or 5010), and number of DRAM and Data Buffers placed.
6. See PMIC supplier datasheet for Minimum and Maximum ratings.

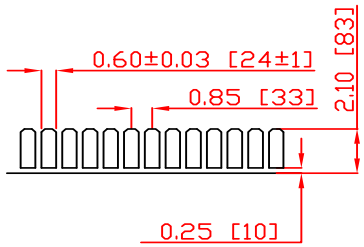
Mechanical Drawing

Unit: mm





Detail A



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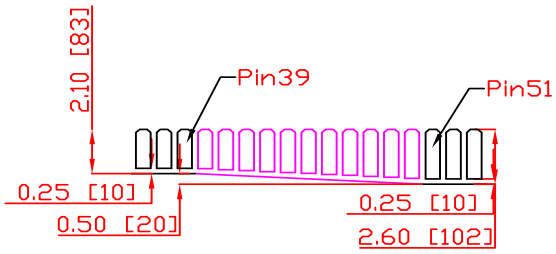

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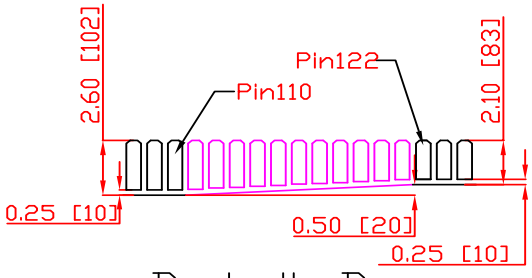

Detail D

30µ inch gold finger

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
1.0	4/12/2022	Initial release	

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