

RoHS Compliant

8GB REGISTERED DDR3 DIMM

Product Specifications

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Version 1.1



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General Description

Apacer **78.C1GEZ.4010C** is a 1024M x 72 DDR3 SDRAM (Synchronous DRAM) ECC Registered DIMM. This high-density memory module consists of 18 pieces 512M x 8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 240-pins dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

Ordering Information

| Part Number | Bandwidth | Speed Grade | Max Frequency | CAS Latency |
|----------------|-------------|-------------|---------------|-------------|
| 78.C1GEZ.4010C | 10.6 GB/sec | 1333 Mbps | 666 MHz | CL9 |

| Density | Organization | Component | Rank |
|---------|--------------|------------|------|
| 8GB | 1024M x 72 | 512M x8*18 | 2 |

Key Parameters

| MT/s | DDR3-1066 | DDR3-1333 | DDR3-1600 | DDR3-1866 | Unit |
|-------------|-----------|-----------|-----------|-----------|------|
| Grade | -CL7 | -CL9 | -CL11 | -CL13 | |
| tCK (min) | 1.875 | 1.5 | 1.25 | 1.071 | ns |
| CAS latency | 7 | 9 | 11 | 13 | tCK |
| tRCD (min) | 13.125 | 13.5 | 13.75 | 13.91 | ns |
| tRP (min) | 13.125 | 13.5 | 13.75 | 13.91 | ns |
| tRAS (min) | 37.5 | 36 | 35 | 34 | ns |
| tRC (min) | 50.625 | 49.5 | 48.75 | 47.91 | ns |
| CL-tRCD-tRP | 7-7-7 | 9-9-9 | 11-11-11 | 13-13-13 | tCK |

Specifications:

- ◆ Support ECC error detection and correction
- ◆ On-DIMM thermal sensor : Yes
- ◆ Organization: 1024 words x 72 bits, 2 ranks
- ◆ Integrating 18 pieces of 4G bits DDR3 SDRAM sealed FBGA
- ◆ Package: 240-pin socket type dual in-line memory module (REG DIMM)
- ◆ PCB: height 30.0 mm, lead pitch 1.0 mm (pin), lead-free (RoHS compliant)
- ◆ Power supply VDD: 1.5V ± 0.075V
- ◆ Serial Presence Detect (SPD)
- ◆ Eight Internal banks for concurrent operation
- ◆ Interface: SSTL_15
- ◆ Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- ◆ CAS Latency (CL): 6, 7, 8, 9
- ◆ CAS Write Latency (CWL): 5, 6, 7
- ◆ Supports auto pre-charge option for each burst access
- ◆ Supports auto-refresh/self-refresh
- ◆ Refresh cycles: 7.8 μ s at 0°C ≤ TC ≤ +85°C
- ◆ PCB: 30 μ gold finger

Features:

- ◆ Double-data-rate architecture: 2 data transfers per clock cycle
- ◆ The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- ◆ Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- ◆ DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- ◆ Differential clock inputs (CK and /CK)
- ◆ DLL aligns DQ and DQS transitions with CK transitions
- ◆ Data mask (DM) for writing data
- ◆ Posted /CAS by programmable additive latency for enhanced command and data bus efficiency
- ◆ On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- ◆ Multi-Purpose Register (MPR) for temperature read out
- ◆ ZQ calibration for DQ drive and ODT
- ◆ Programmable Partial Array Self-Refresh (PASR)
- ◆ /Reset pin for power-up sequence and reset function
- ◆ SRT range: normal/extended, auto/manual self-refresh
- ◆ Programmable output driver impedance control
- ◆ Commands entered at each positive clock input, while data and data mask are referenced to both edges of DQS

Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|--------------------------|---------|----------------------------------|---------|-----------------------------|---------|--------------------------|
| 1 | VREFDQ | 31 | DQ25 | 61 | A2 | 91 | DQ41 |
| 2 | Vss | 32 | Vss | 62 | VDD | 92 | Vss |
| 3 | DQ0 | 33 | $\overline{\text{DQS3}}$ | 63 | CK1,NC | 93 | $\overline{\text{DQS5}}$ |
| 4 | DQ1 | 34 | DQS3 | 64 | $\overline{\text{CK1}}$,NC | 94 | DQS5 |
| 5 | Vss | 35 | Vss | 65 | VDD | 95 | Vss |
| 6 | $\overline{\text{DQS0}}$ | 36 | DQ26 | 66 | VDD | 96 | DQ42 |
| 7 | DQS0 | 37 | DQ27 | 67 | VREFCA | 97 | DQ43 |
| 8 | VSS | 38 | Vss | 68 | Par_In,NC | 98 | Vss |
| 9 | DQ2 | 39 | CB0,NC | 69 | VDD | 99 | DQ48 |
| 10 | DQ3 | 40 | CB1,NC | 70 | A10,AP | 100 | DQ49 |
| 11 | Vss | 41 | Vss | 71 | BA0 | 101 | Vss |
| 12 | DQ8 | 42 | $\overline{\text{DQS8}}$ | 72 | VDD | 102 | $\overline{\text{DQS6}}$ |
| 13 | DQ9 | 43 | DQS8 | 73 | $\overline{\text{WE}}$ | 103 | DQS6 |
| 14 | Vss | 44 | Vss | 74 | $\overline{\text{CAS}}$ | 104 | Vss |
| 15 | $\overline{\text{DQS1}}$ | 45 | CB2,NC | 75 | VDD | 105 | DQ50 |
| 16 | DQS1 | 46 | CB3,NC | 76 | $\overline{\text{S1}}$,NC | 106 | DQ51 |
| 17 | Vss | 47 | Vss | 77 | ODT1,NC | 107 | Vss |
| 18 | DQ10 | 48 | VTT,NC | 78 | VDD | 108 | DQ56 |
| 19 | DQ11 | 49 | VTT,NC | 79 | $\overline{\text{S2}}$,NC | 109 | DQ57 |
| 20 | Vss | 50 | CKE0 | 80 | Vss | 110 | Vss |
| 21 | DQ16 | 51 | VDD | 81 | DQ32 | 111 | $\overline{\text{DQS7}}$ |
| 22 | DQ17 | 52 | BA2 | 82 | DQ33 | 112 | DQS7 |
| 23 | Vss | 53 | $\overline{\text{Err_out}}$,NC | 83 | Vss | 113 | Vss |
| 24 | $\overline{\text{DQS2}}$ | 54 | VDD | 84 | $\overline{\text{DQS4}}$ | 114 | DQ58 |
| 25 | DQS2 | 55 | A11 | 85 | DQS4 | 115 | DQ59 |
| 26 | Vss | 56 | A7 | 86 | Vss | 116 | Vss |
| 27 | DQ18 | 57 | VDD | 87 | DQ34 | 117 | SA0 |
| 28 | DQ19 | 58 | A5 | 88 | DQ35 | 118 | SCL |
| 29 | Vss | 59 | A4 | 89 | Vss | 119 | SA2 |
| 30 | DQ24 | 60 | VDD | 90 | DQ40 | 120 | VTT |

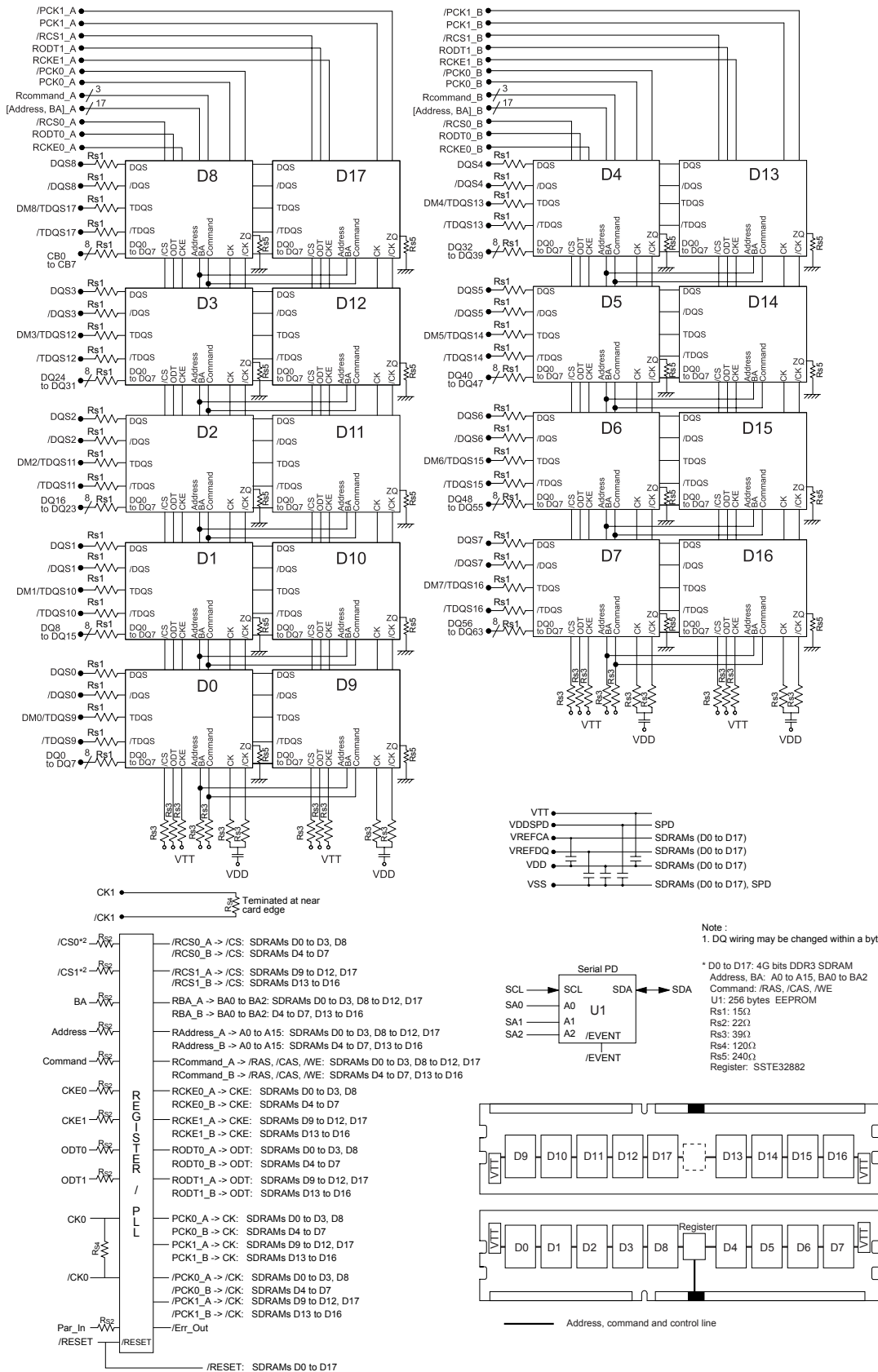
| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|--------------|---------|--------------|---------|--------------|---------|--------------|
| 121 | Vss | 151 | Vss | 181 | A1 | 211 | Vss |
| 122 | DQ4 | 152 | DM3,(T)DQS12 | 182 | VDD | 212 | DM5,(T)DQS14 |
| 123 | DQ5 | 153 | NC, (T)DQS12 | 183 | VDD | 213 | NU, (T)DQS14 |
| 124 | Vss | 154 | Vss | 184 | CK0 | 214 | Vss |
| 125 | DM0,(T)DQS9 | 155 | DQ30 | 185 | CK0 | 215 | DQ46 |
| 126 | NC, (T)DQS9 | 156 | DQ31 | 186 | VDD | 216 | DQ47 |
| 127 | Vss | 157 | Vss | 187 | EVENT ,NC | 217 | Vss |
| 128 | DQ6 | 158 | CB4,NC | 188 | A0 | 218 | DQ52 |
| 129 | DQ7 | 159 | CB5,NC | 189 | VDD | 219 | DQ53 |
| 130 | Vss | 160 | VSS | 190 | BA1 | 220 | Vss |
| 131 | DQ12 | 161 | DM8(T)DQS17 | 191 | VDD | 221 | DM6,(T)DQS15 |
| 132 | DQ13 | 162 | NC, (T)DQS17 | 192 | RAS | 222 | NC, (T)DQS15 |
| 133 | Vss | 163 | Vss | 193 | S0 | 223 | Vss |
| 134 | DM1,(T)DQS10 | 164 | CB6,NC | 194 | VDD | 224 | DQ54 |
| 135 | NC, (T)DQS10 | 165 | CB7,NC | 195 | ODT0 | 225 | DQ55 |
| 136 | Vss | 166 | Vss | 196 | A13 | 226 | Vss |
| 137 | DQ14 | 167 | NC(TEST) | 197 | VDD | 227 | DQ60 |
| 138 | DQ15 | 168 | RESET | 198 | S3 ,NC | 228 | DQ61 |
| 139 | Vss | 169 | CKE1,NC | 199 | Vss | 229 | Vss |
| 140 | DQ20 | 170 | VDD | 200 | DQ36 | 230 | DM7(T)DQS16 |
| 141 | DQ21 | 171 | NC,A15 | 201 | DQ37 | 231 | NC, (T)DQS16 |
| 142 | Vss | 172 | NC,A14 | 202 | Vss | 232 | Vss |
| 143 | DM2(T)DQS11 | 173 | VDD | 203 | DM4,(T)DQS13 | 233 | DQ62 |
| 144 | NC, (T)DQS11 | 174 | A12 | 204 | NC, (T)DQS13 | 234 | DQ63 |
| 145 | Vss | 175 | A9 | 205 | Vss | 235 | Vss |
| 146 | DQ22 | 176 | VDD | 206 | DQ38 | 236 | VDDSPD |
| 147 | DQ23 | 177 | A8 | 207 | DQ39 | 237 | SA1 |
| 148 | Vss | 178 | A6 | 208 | Vss | 238 | SDA |
| 149 | DQ28 | 179 | VDD | 209 | DQ44 | 239 | Vss |
| 150 | DQ29 | 180 | A3 | 210 | DQ45 | 240 | VTT |

*IC Component Composition : 256Mx8 A0~A14 256Mx4 A0~A13
 512Mx8 A0~A15 512Mx4 A0~A14
 1024Mx8 A0~A15 1024Mx4 A0~A15

Pin Descriptions

| Pin Name | Description |
|-----------------------------------|---|
| Ax* | SDRAM address bus |
| BAx | SDRAM bank select |
| DQx | DIMM memory data bus |
| CBx | DIMM ECC check bits |
| $\overline{\text{RAS}}$ | SDRAM row address strobe |
| $\overline{\text{CAS}}$ | SDRAM column address strobe |
| $\overline{\text{WE}}$ | SDRAM write enable |
| $\overline{\text{Sx}}$ | SDRAM Chip select lines |
| CKEx | SDRAM clock enable lines |
| CKx | SDRAM clock input |
| $\overline{\text{CKx}}$ | SDRAM Differential clock input |
| DQSx | SDRAM data strobes(positive line of differential pair) |
| $\overline{\text{DQSx}}$ | SDRAM data strobes(negative line of differential pair) |
| TDQSx ; $\overline{\text{TDQSx}}$ | Termination data strobe |
| DMx | SDRAM input mask |
| SCL | Clock input for serial PD |
| SDA | Data input/output for serial PD |
| SAX | Serial address input |
| VDD | Power for internal circuit |
| VDDSPD | Serial EEPROM positive power supply |
| VREFDQ | SDRAM I/O reference supply |
| VREFCA | SDRAM command/address reference supply |
| VSS | Power supply return(ground) |
| VTT | SDRAM I/O termination supply |
| $\overline{\text{RESET}}$ | Set DRAM to known state |
| ODTx | On-die termination control lines |
| Par_In | Parity bit for the Address and Control bus |
| $\overline{\text{Err_Out}}$ | Parity error found on the Address and Control bus |
| $\overline{\text{EVENT}}$ | An output of the thermal sensor to indicate critical module temperature |
| NC | Spare pins(no connect) |
| TEST | Reserved for optional hardware temperature sensing |

Functional Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Description | Units |
|-------------------------------------|-------------------|-------------------|-------|
| Voltage on VDD pin relative to Vss | V_{DD} | - 0.4 V ~ 1.975 V | V |
| Voltage on VDDQ pin relative to Vss | V_{DDQ} | - 0.4 V ~ 1.975 V | V |
| Voltage on any pin relative to Vss | V_{IN}, V_{OUT} | - 0.4 V ~ 1.975 V | V |
| Storage Temperature | TSTG | -55 to +100 | °C |

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|-------------------|------------------------------------|----------|-------|-------|
| T _{OPER} | Normal Operating Temperature Range | 0 to 85 | °C | 1,2 |
| | Extended Temperature Range | 85 to 95 | °C | 1,3 |

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For Measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating Conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range.
 - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Operating Conditions

Recommended DC Operating Conditions - DDR3 (1.5V) operation

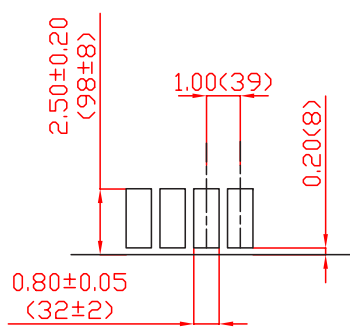
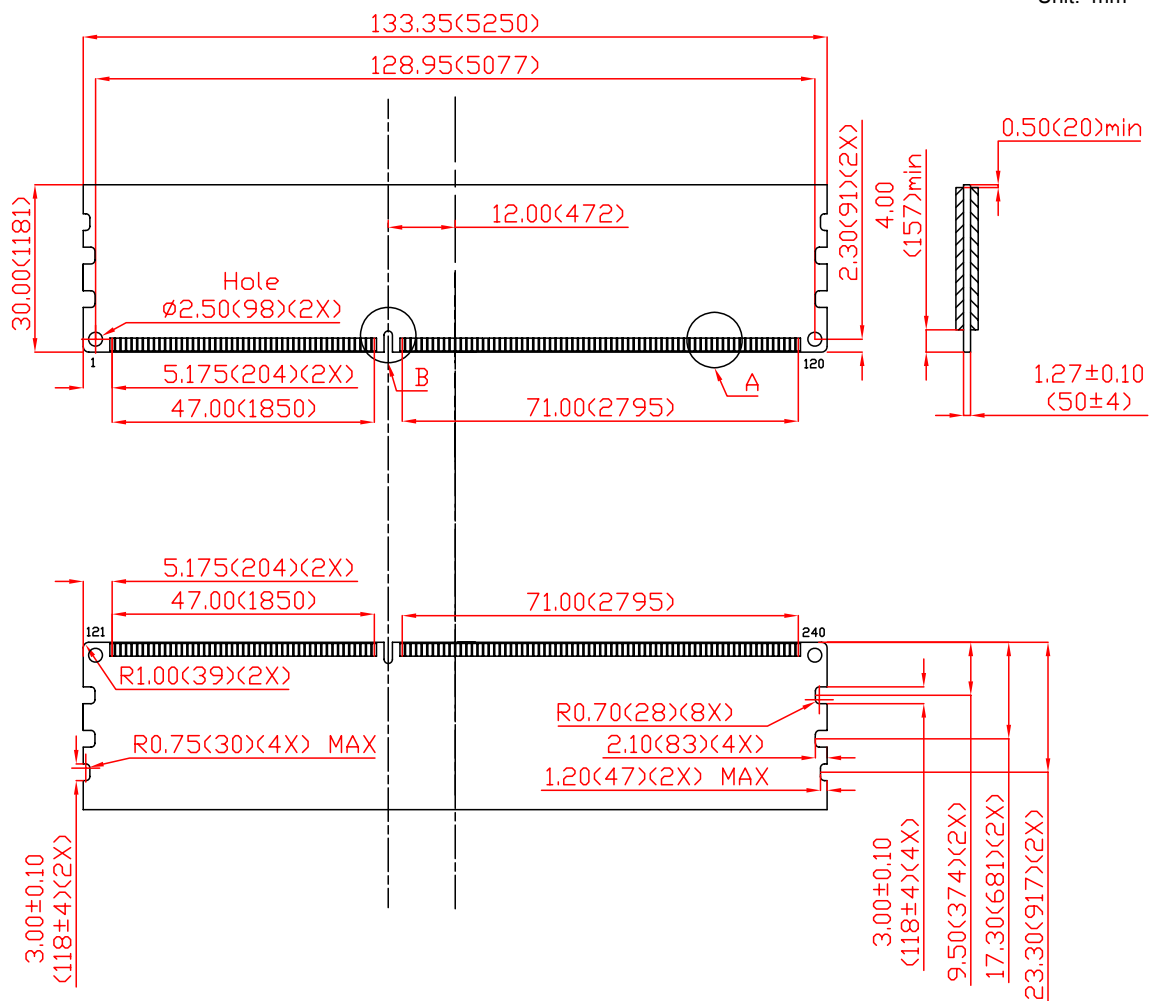
| Symbol | Parameter | Rating | | | Units |
|--------|---------------------------|--------|------|-------|-------|
| | | Min. | Typ. | Max. | |
| VDD | Supply Voltage | 1.425 | 1.5 | 1.575 | V |
| VDDQ | Supply Voltage for Output | 1.425 | 1.5 | 1.575 | V |

Notes:

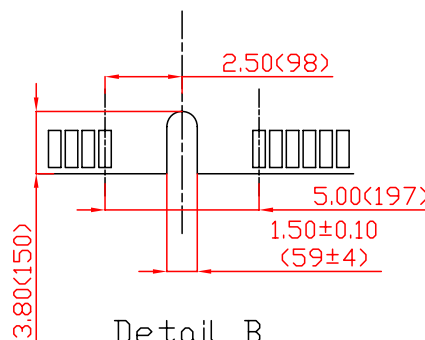
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Mechanical Drawing

Unit: mm



Detail A



Detail B

30μ gold finger

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

| Revision | Date | Description | Remark |
|-----------------|-------------|---|---------------|
| 0.9 | 08/28/2012 | Official release | |
| 1.0 | 08/29/2012 | release | |
| 1.1 | 07/23/2013 | 1.Changed headquarters address 2.Added 30μ gold finger | |

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