

Apacer Memory Product Specification

2048MB DDR2 DIMM

2GB DDR2 DIMM based on 128MX8 ,8Banks, 1.8V DDR2 DIMM with SPD

Features

• Performance range (Bandwidth: 5.3 GB/sec)

Part Number	Max Freq. (Clock)	Speed Grade
78.A1G9O.404	333MHz(3ns@CL5)	667Mbps

- JEDEC standard 1.8V $\pm$ 0.1V Power Supply
- VDDQ = 1.8V $\pm$ 0.1V
- Internal Bank: 8 Bank
- Posted CAS
- Programmable CAS Latency: 4, 5, 6
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Refresh and Self Refresh
Average Refresh Period 7.8us
- Serial presence detect with EEPROM
- Compliance with RoHS
- Compliance with CE
- Operating Temperature Range:
• Commercial $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
- Refresh: auto-refresh, self-refresh
• —Average refresh period
7.8us at $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
3.9us at $85^{\circ}\text{C} \leq \text{TC} \leq 95^{\circ}\text{C}$

Pin Description

Pin Name	Description	Pin Name	Description
A0-A13	DDR2 SDRAM address bus	CK0, CK1, CK2	DDR2 SDRAM clocks (positive line of differential pair)
BA0-BA2	DDR2 SDRAM bank select	$\overline{\text{CK0}}, \overline{\text{CK1}}, \overline{\text{CK2}}$	DDR2 SDRAM clocks (negative line of differential pair)
$\overline{\text{RAS}}$	DDR2 SDRAM row address strobe	SCL	I ² C serial bus clock for EEPROM
$\overline{\text{CAS}}$	DDR2 SDRAM column address strobe	SDA	I ² C serial bus data line for EEPROM
$\overline{\text{WE}}$	DDR2 SDRAM write enable	SA0-SA2	I ² C serial address select for EEPROM
$\overline{\text{S0}}, \overline{\text{S1}}$	DIMM Rank Select Lines	V _{DD} *	DDR2 SDRAM core power supply
CKE0,CKE1	DDR2 SDRAM clock enable lines	V _{DDQ} *	DDR2 SDRAM I/O Driver power supply
ODT0, ODT1	On-die termination control lines	V _{REF}	DDR2 SDRAM I/O reference supply
DQ0 - DQ63	DIMM memory data bus	V _{SS}	Power supply return (ground)
CB0 - CB7	DIMM ECC check bits	V _{DD} SPD	Serial EEPROM positive power supply
DQS0 - DQS8	DDR2 SDRAM data strobes	NC	Spare Pins(no connect)
DM(0-8)	DDR2 SDRAM data masks	RESET	Not used on UDIMM
$\overline{\text{DQS0}}\text{-}\overline{\text{DQS8}}$	DDR2 SDRAM differential data strobes	TEST	Used by memory bus analysis tools (unused on memory DIMMs)

*The VDD and VDDQ pins are tied to the single power-plane on PCB.

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Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REF}	121	V _{SS}	31	DQ19	151	V _{SS}	61	A4	181	V _{DDQ}	91	V _{SS}	211	DM5
2	V _{SS}	122	DQ4	32	V _{SS}	152	DQ28	62	V _{DDQ}	182	A3	92	$\overline{\text{DQS}}5$	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V _{SS}
4	DQ1	124	V _{SS}	34	DQ25	154	V _{SS}	64	V _{DD}	184	V _{DD}	94	V _{SS}	214	DQ46
5	V _{SS}	125	DM0	35	V _{SS}	155	DM3	KEY				95	DQ42	215	DQ47
6	$\overline{\text{DQS}}0$	126	NC	36	$\overline{\text{DQS}}3$	156	NC	65	V _{SS}	185	CK0	96	DQ43	216	V _{SS}
7	DQS0	127	V _{SS}	37	DQS3	157	V _{SS}	66	V _{SS}	186	$\overline{\text{CK}}0$	97	V _{SS}	217	DQ52
8	V _{SS}	128	DQ6	38	V _{SS}	158	DQ30	67	V _{DD}	187	V _{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC	188	A0	99	DQ49	219	V _{SS}
10	DQ3	130	V _{SS}	40	DQ27	160	V _{SS}	69	V _{DD}	189	V _{DD}	100	V _{SS}	220	CK2
11	V _{SS}	131	DQ12	41	V _{SS}	161	NC	70	A10/AP	190	BA1	101	SA2	221	$\overline{\text{CK}}2$
12	DQ8	132	DQ13	42	NC	162	NC	71	BA0	191	V _{DDQ}	102	NC, TEST ²	222	V _{SS}
13	DQ9	133	V _{SS}	43	NC	163	V _{SS}	72	V _{DDQ}	192	$\overline{\text{RAS}}$	103	V _{SS}	223	DM6
14	V _{SS}	134	DM1	44	V _{SS}	164	NC	73	$\overline{\text{WE}}$	193	$\overline{\text{S}}0$	104	$\overline{\text{DQS}}6$	224	NC
15	$\overline{\text{DQS}}1$	135	NC	45	NC	165	NC	74	$\overline{\text{CAS}}$	194	V _{DDQ}	105	DQS6	225	V _{SS}
16	DQS1	136	V _{SS}	46	NC	166	V _{SS}	75	V _{DDQ}	195	ODT0	106	V _{SS}	226	DQ54
17	V _{SS}	137	CK1	47	V _{SS}	167	NC	76	$\overline{\text{S}}1$	196	NC/A13	107	DQ50	227	DQ55
18	NC	138	$\overline{\text{CK}}1$	48	NC	168	NC	77	ODT1	197	V _{DD}	108	DQ51	228	V _{SS}
19	NC	139	V _{SS}	49	NC	169	V _{SS}	78	V _{DDQ}	198	V _{SS}	109	V _{SS}	229	DQ60
20	V _{SS}	140	DQ14	50	V _{SS}	170	V _{DDQ}	79	V _{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V _{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V _{SS}
22	DQ11	142	V _{SS}	52	CKE0	172	V _{DD}	81	DQ33	201	V _{SS}	112	V _{SS}	232	DM7
23	V _{SS}	143	DQ20	53	V _{DD}	173	NC	82	V _{SS}	202	DM4	113	$\overline{\text{DQS}}7$	233	NC
24	DQ16	144	DQ21	54	BA2	174	NC	83	$\overline{\text{DQS}}4$	203	NC	114	DQS7	234	V _{SS}
25	DQ17	145	V _{SS}	55	NC	175	V _{DDQ}	84	DQS4	204	V _{SS}	115	V _{SS}	235	DQ62
26	V _{SS}	146	DM2	56	V _{DDQ}	176	A12	85	V _{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{\text{DQS}}2$	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V _{SS}
28	DQS2	148	V _{SS}	58	A7	178	V _{DD}	87	DQ35	207	V _{SS}	118	V _{SS}	238	VDDSPD
29	V _{SS}	149	DQ22	59	V _{DD}	179	A8	88	V _{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V _{SS}				

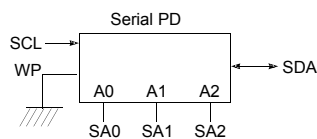
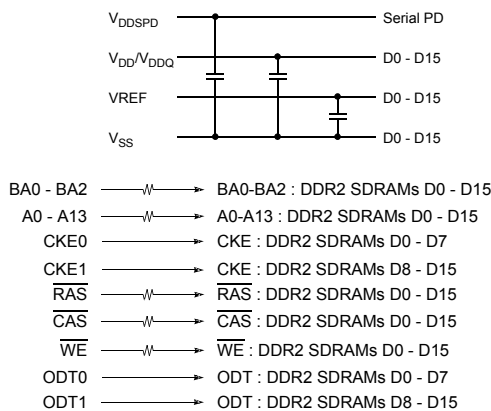
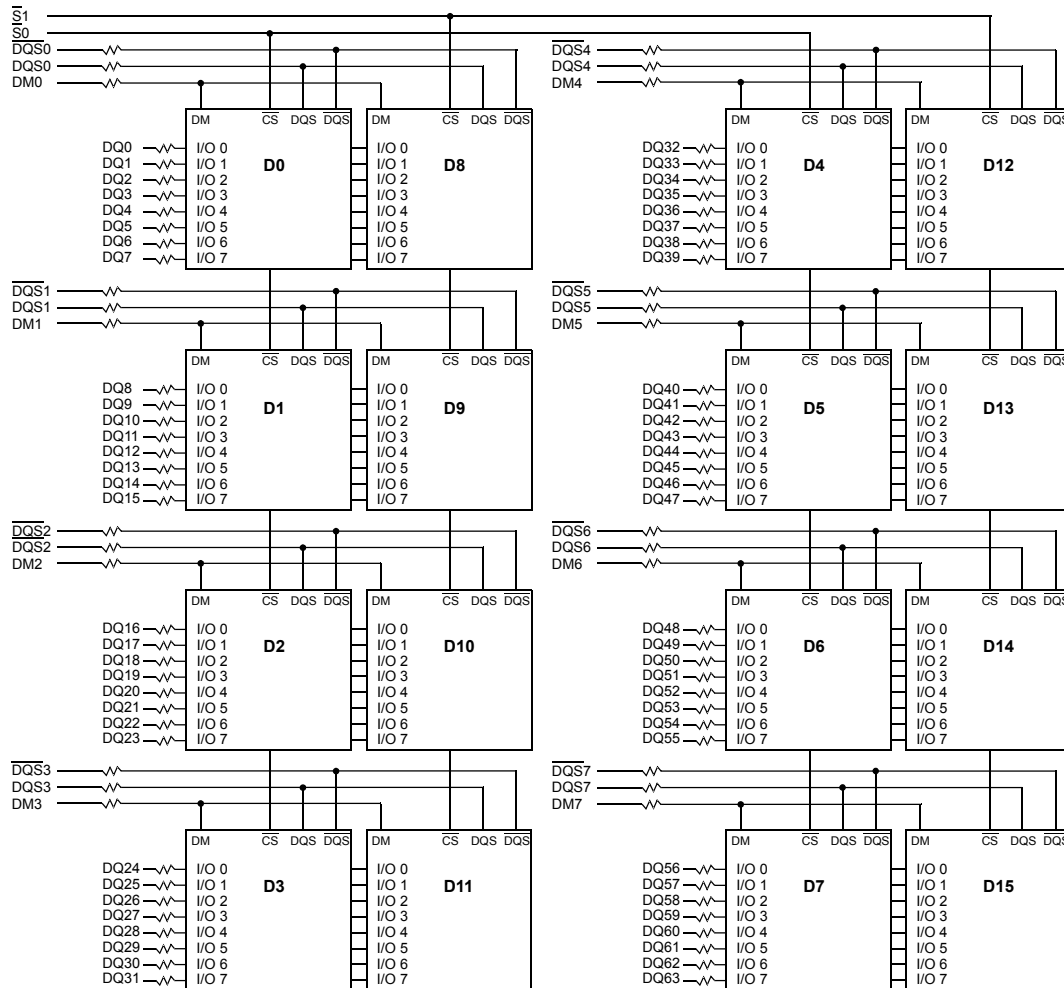
NC = No Connect, RFU = Reserved for Future Use

1. Pin173 Pin174 are reserved for 2Gb/4Gb comp. base Unbuffered DIMM.

2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

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Function Block Diagram



* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	4 DDR2 SDRAMs
*CK1/CK1	6 DDR2 SDRAMs
*CK2/CK2	6 DDR2 SDRAMs

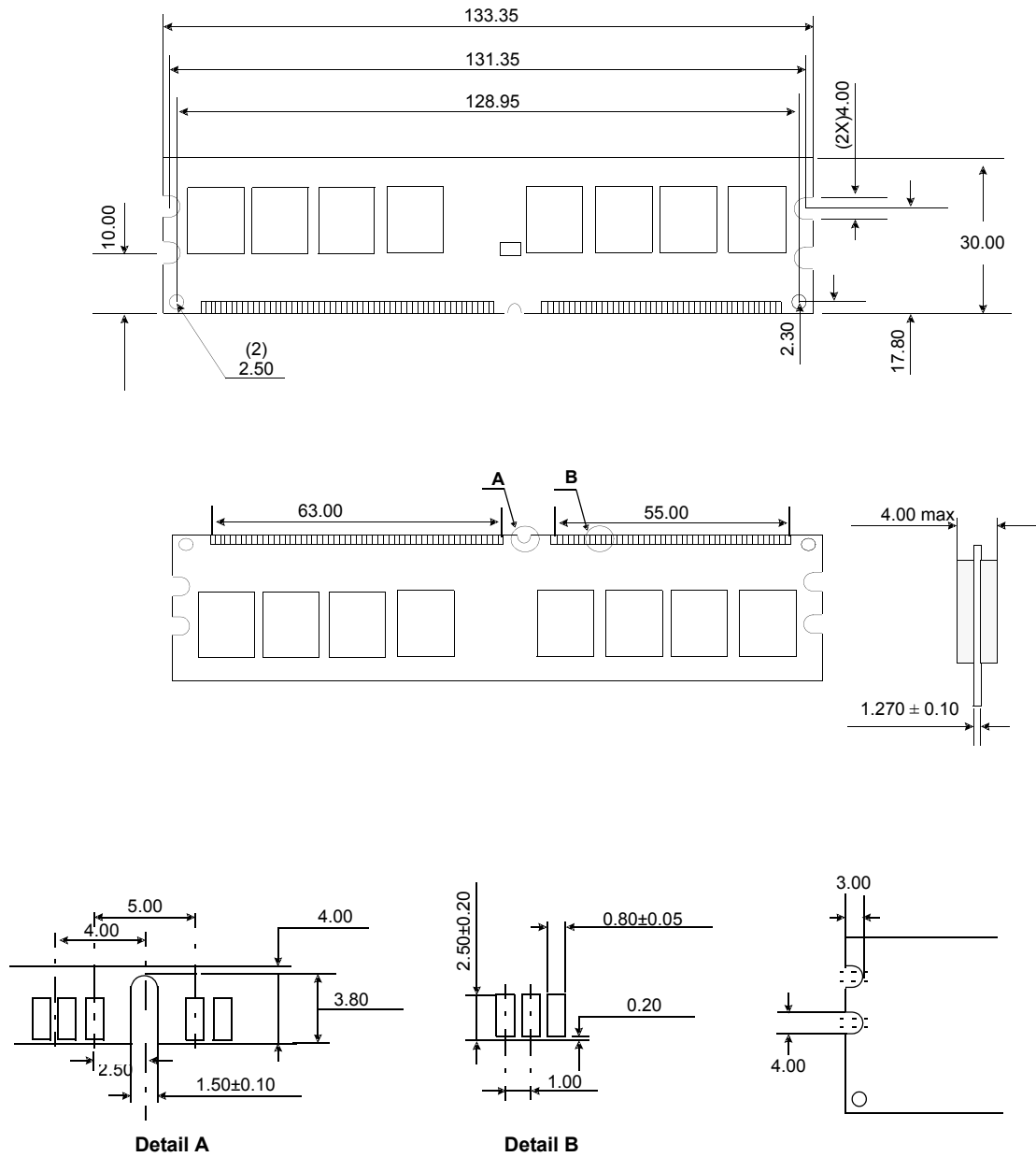
*Wire per Clock Loading Table/Wiring Diagrams

Notes :

1. DQ, DM, DQS/DQS-bar resistors : 22 Ohms " 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 3 Ohms " 5%.

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PACKAGE DIMENSIONS



Tolerances: +0.15mm unless otherwise specified