1024MB DDR SDRAM SO-DIMM

1024M DDR SDRAM SO-DIMM based on 64MX8, 4Banks, 2.6V DDR SDRAM with SPD

Features

.Performance range (Bandwidth: 3.2 GB/sec)

Part No.	Max Freq. (Clock)	Speed Grade
75.063AS.G030C	200MHz(5ns@CL3)	400 Mbps

- Power supply Vdd: 2.6V +/-0.1V
- MRS cycle with address key programs
- CAS Latency (Access from column address):2.5,3
- Burst length ;2, 4, 8
- Data scramble ;Sequential & Interleave
- Serial presence detect with EEPROM
- SSTL-2 interface
- Differential clock input
- Compliance With RoHS
- Compliance With CE
- Auto Refresh and self Refresh Modes
  64ms, 8192-cycle refresh
- Operating Temperature Range:
- Industrial -40°C ≦ TA ≦ 85°C
- Industrial System Level -40°C ≦ TA ≦ 70°C

Description

This module is 128M bit x 64 Double Data Rate SDRAM high density memory modules based on first generation of 512Mb DDR SDRAM respectively.

It consists of sixteen CMOS 64M x8 bit with 4banks Double Data Rate SDRAMs in FBGA 60 ball packages mounted on a 200pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Pin Description:

Symbol	Type	Polarity	Function
CK0 - CK2, $\overline{CK0}$ - $\overline{CK2}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$0, $\overline{S}$1	Input	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S}$0; Bank 1 is selected by $\overline{S}$1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0 - BA1	Input	—	Selects which DDR SDRAM bank of four is activated.
A0 - A9, A11-A12 A10/AP	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	In/Out	—	Data Bit Input/Output pins.
CB0 - CB7	In/Out	—	Data Check Bit Input/Output pins. Not used on x64 modules.
DM0 - DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
DQS0 - DQS8	In/Out	—	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR SDRAMs and is sent at the leading edge of the data window. DQS8 is associated with check bits CB0-CB7, and is not used on x64 modules.
V_{DD}, V_{DD}SPD, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
V_{DD}ID	Out	—	Defines relationship of V_{DD} and V_{DD}Q. If V_{DD}ID is open, V_{DD} = V_{DD}Q; if V_{DD}ID is pulled to V_{SS}, $V_{DD} \neq V_{DD}$Q. This line should be pulled high through 10 KΩ on the host board.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.
SA0 - SA2	Input	—	Address pins used to select the Serial Presence Detect.

Pinout:

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V_{SS}	4	V_{SS}	53	DQ19	54	DQ23	103	V_{SS}	104	V_{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V_{DD}	156	V_{DD}
7	DQ1	8	DQ5	57	V_{DD}	58	V_{DD}	107	A5	108	A4	157	V_{DD}	158	$\overline{CK}1$
9	V_{DD}	10	V_{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V_{SS}	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V_{SS}	162	V_{SS}
13	DQ2	14	DQ6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ48	164	DQ52
15	V_{SS}	16	V_{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	$\overline{RAS}$	167	V_{DD}	168	V_{DD}
19	DQ8	20	DQ12	69	V_{DD}	70	V_{DD}	119	$\overline{WE}$	120	$\overline{CAS}$	169	DQS6	170	DM6
21	V_{DD}	22	V_{DD}	71	CB0	72	CB4	121	$\overline{S}0$	122	$\overline{S}1$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	DU	124	DU	173	V_{SS}	174	V_{SS}
25	DQS1	26	DM1	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	V_{DD}	180	V_{DD}
31	DQ11	32	DQ15	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ57	182	DQ61
33	V_{DD}	34	V_{DD}	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	V_{DD}	85	DU	86	$\overline{DU}$ ($\overline{RESET}$)	135	DQ34	136	DQ38	185	V_{SS}	186	V_{SS}
37	$\overline{CK}0$	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ58	188	DQ62
39	V_{SS}	40	V_{SS}	89	CK2	90	V_{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{CK}2$	92	V_{DD}	141	DQ40	142	DQ44	191	V_{DD}	192	V_{DD}
43	DQ17	44	DQ21	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA0
45	V_{DD}	46	V_{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU (A13)	98	DU (BA2)	147	DQS5	148	DM5	197	V_{DD}SPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V_{SS}	150	V_{SS}	199	V_{DD}ID	200	DU

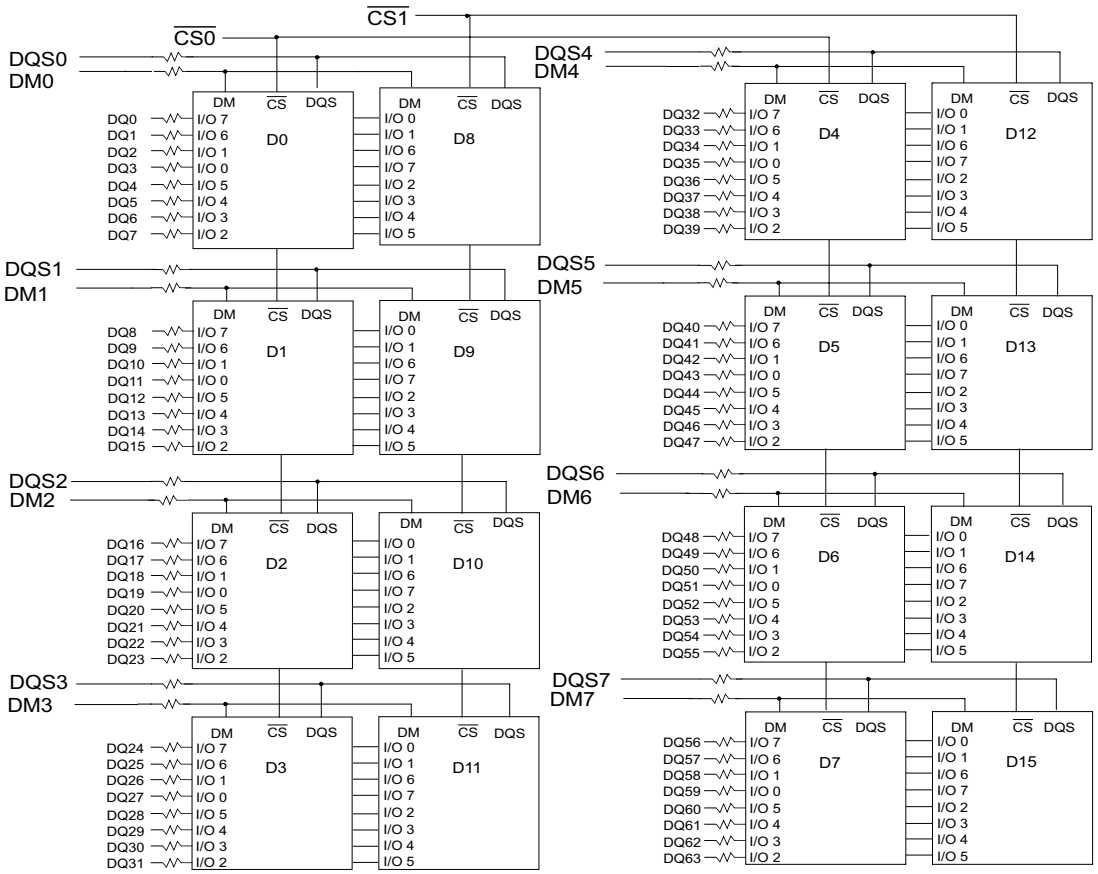
Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.

Note: Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.

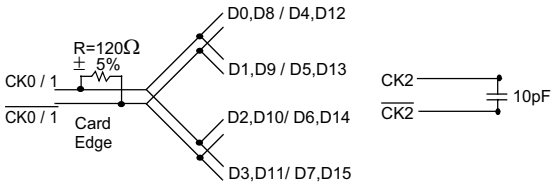
Note: Pins 89, 91are reserved for x72 modules or registered modules.

Note: Pin 97 reserved for higher density memories, requiring A13

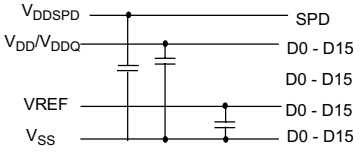
Note: Pin 98 reserved for devices with eight banks, requiring BA2



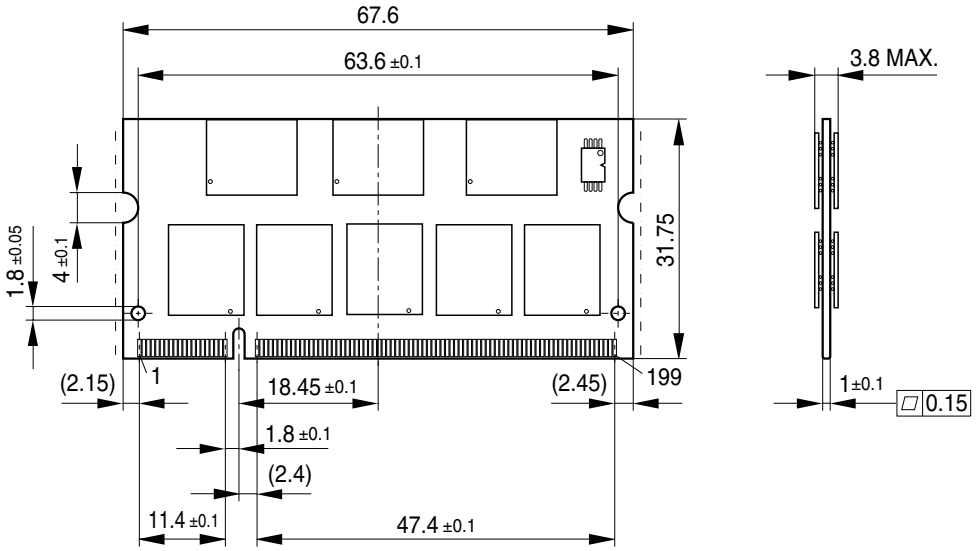
BA0 - BA1	→	BA0-BA1: DDR SDRAMs D0 - D15
A0 - A12	→	A0-A12 : DDR SDRAMs D0 - D15
$\overline{RAS}$	→	$\overline{RAS}$: DDR SDRAMs D0 - D15
$\overline{CAS}$	→	$\overline{CAS}$: DDR SDRAMs D0 - D15
CKE1	→	CKE : DDR SDRAMs D8 - D15
CKE0	→	CKE : DDR SDRAMs D0 - D7
$\overline{WE}$	→	$\overline{WE}$: DDR SDRAMs D0 - D15

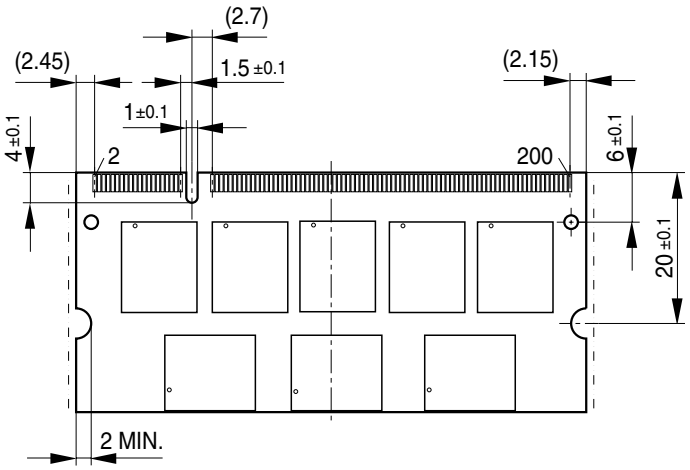


*Clock Net Wiring

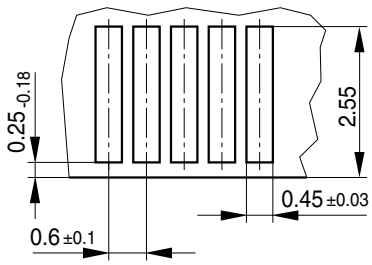


Notes :
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown
3. DQ, DQS, DM/DQS resistors: 22 Ohm.





Detail of contacts



– – – Burnished, no burr allowed

Tolerances:+-0.15mm unless otherwise specified