RoHS Compliant

32GB DDR5 SDRAM UDIMM

Fully lead-free / Halogen free

Product Specifications

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Version 1.2

Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

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General Description

Apacer **D12.35306H.002** is a 32GB DDR5 SDRAM (Synchronous DRAM) DIMM. This memory module consists of 16 pieces 2G x 8 bits DDR5 synchronous DRAMs in FBGA packages and 8K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Density	Speed	Organization	DRAM Composition	Rank
D12.35306H.002	32GB	5600 Mbps	4Gx64	2Gx8 *16	2

Key Parameters

Speed	DDR5-4800	DDR5-5600	Unit
	-CL40	-CL46	
tCK (min)	0.416	0.357	ns
CAS latency	40	46	nCK
tRCD (min)	16	16	ns
tRP (min)	16	16	ns
tRAS (min)	32	32	ns
tRC (min)	48	48	ns
CL-tRCD-tRP	40-39-39	46-45-45	nCK

Features:

- JEDEC standard compliant
- On-DIMM thermal sensor : Yes
- PCB: height 31.25 mm, lead pitch 0.85 mm (pin),
- VDD = VDDQ= 1.1V (1.067V to 1.166V)
- VPP = 1.8V (1.746V to 1.908V)、VDDSPD = 1.8V
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- CAS Latency (CL): 22,26,28,30,32,36,40,42,46,48,50
- CAS Write Latency (CWL): RL-2
- Operating temperature Tcase–(0℃~85℃)
- Average Refresh period 3.9us at lower than Tcase 85°C, 1.95us at 85°C < Tcase < 95 °C.
- All bank and same bank refresh
- Bi-Directional Differential Data Strobe
- 16-bit prefetch architecture
- On-die ECC
- ECC transparency and error scrub
- sPPR and hPPR capability
- Halogen free
- Fully lead-free (RoHS compliant without exemptions)

Pin Assignments

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
1	VIN_BULK	145	VIN_BULK	74	VSS	218	VSS
2	RFU	146	VIN_BULK	75	RFU	219	RFU
3	RFU	147	PWR_ - GOOD	76	RFU	220	RFU
4	HSCL	148	HSA	77	VSS	221	VSS
5	HSDA	149	RFU	78	CK0_B_t	222	CK1_B_t
6	VSS	150	VSS	79	CK0_B_c	223	CK1_B_c
7	RFU	151	PWR_EN	80	VSS	224	VSS
8	VSS	152	RFU	81	RFU	225	RFU
9	DQ0_A	153	VSS	82	CA12_B	226	RFU
10	VSS	154	DQ2_A	83	VSS	227	VSS
11	DQ1_A	155	VSS	84	CA10_B	228	CA11_B
12	VSS	156	DQ3_A	85	CA8_B	229	CA9_B
13	DQS0_A_c	157	VSS	86	VSS	230	VSS
14	DQS0_A_t	158	DM0_A_n	87	CA6_B	231	CA7_B
15	VSS	159	VSS	88	CA4_B	232	CA5_B
16	DQ4_A	160	DQ6_A	89	VSS	233	VSS
17	VSS	161	VSS	90	CA2_B	234	CA3_B
18	DQ5_A	162	DQ7_A	91	CA0_B	235	CA1_B
19	VSS	163	VSS	92	VSS	236	VSS
20	DQ8_A	164	DQ10_A	93	CS0_B_n	237	CS1_B_n
21	VSS	165	VSS	94	VSS	238	VSS
22	DQ9_A	166	DQ11_A	95	RESET_n	239	DQS4_B_c
23	VSS	167	VSS	96	VSS	240	DQS4_B_t
24	DM1_A_n	168	DQS1_A_c	97	CB0_B	241	VSS
25	VSS	169	DQS1_A_t	98	VSS	242	CB2_B
26	DQ12_A	170	VSS	99	CB1_B	243	VSS
27	VSS	171	DQ14_A	100	VSS	244	CB3_B
28	DQ13_A	172	VSS	101	DQ0_B	245	VSS
29	VSS	173	DQ15_A	102	VSS	246	DQ2_B
30	DQ16_A	174	VSS	103	DQ1_B	247	VSS
31	VSS	175	DQ18_A	104	VSS	248	DQ3_B
32	DQ17_A	176	VSS	105	DQS0_B_c	249	VSS
33	VSS	177	DQ19_A	106	DQS0_B_t	250	DM0_B_n
34	DQS2_A_c	178	VSS	107	VSS	251	VSS
35	DQS2_A_t	179	DM2_A_n	108	DQ4_B	252	DQ6_B
36	VSS	180	VSS	109	VSS	253	VSS
37	DQ20_A	181	DQ22_A	110	DQ5_B	254	DQ7_B
38	VSS	182	VSS	111	VSS	255	VSS
39	DQ21_A	183	DQ23_A	112	DQ8_B	256	DQ10_B

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
40	VSS	184	VSS	113	VSS	257	VSS
41	DQ24_A	185	DQ26_A	114	DQ9_B	258	DQ11_B
42	VSS	186	VSS	115	VSS	259	VSS
43	DQ25_A	187	DQ27_A	116	DM1_B_n	260	DQS1_B_c
44	VSS	188	VSS	117	VSS	261	DQS1_B_t
45	DM3_A_n	189	DQS3_A_c	118	DQ12_B	262	VSS
46	VSS	190	DQS3_A_t	119	VSS	263	DQ14_B
47	DQ28_A	191	VSS	120	DQ13_B	264	VSS
48	VSS	192	DQ30_A	121	VSS	265	DQ15_B
49	DQ29_A	193	VSS	122	DQ16_B	266	VSS
50	VSS	194	DQ31_A	123	VSS	267	DQ18_B
51	CB0_A	195	VSS	124	DQ17_B	268	VSS
52	VSS	196	CB2_A	125	VSS	269	DQ19_B
53	CB1_A	197	VSS	126	DQS2_B_c	270	VSS
54	VSS	198	CB3_A	127	DQS2_B_t	271	DM2_B_n
55	DQS4_A_c	199	VSS	128	VSS	272	VSS
56	DQS4_A_t	200	ALERT_n	129	DQ20_B	273	DQ22_B
57	VSS	201	VSS	130	VSS	274	VSS
58	CS0_A_n	202	CS1_A_n	131	DQ21_B	275	DQ23_B
59	VSS	203	VSS	132	VSS	276	VSS
60	CA0_A	204	CA1_A	133	DQ24_B	277	DQ26_B
61	CA2_A	205	CA3_A	134	VSS	278	VSS
62	VSS	206	VSS	135	DQ25_B	279	DQ27_B
63	CA4_A	207	CA5_A	136	VSS	280	VSS
64	CA6_A	208	CA7_A	137	DM3_B_n	281	DQS3_B_c
65	VSS	209	VSS	138	VSS	282	DQS3_B_t
66	CA8_A	210	CA9_A	139	DQ28_B	283	VSS
67	CA10_A	211	CA11_A	140	VSS	284	DQ30_B
68	VSS	212	VSS	141	DQ29_B	285	VSS
69	CA12_A	213	RFU	142	VSS	286	DQ31_B
70	RFU	214	RFU	143	RFU	287	VSS
71	VSS	215	VSS	144	RFU	288	RFU
72	CK0_A_t	216	CK1_A_t				
73	CK0_A_c	217	CK1_A_c				

Pin Descriptions

Pin Name	Descripti
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits (Only applicable on ECC SODIMM or ECC UDIMM)
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)
HSCL	Side Band bus clock
HSDA	Side Band bus data
HSA	Side Band bus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a Known State
VIN_BULK	5 V power input supply to the PMIC for analog circuits
VSS	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

*Notes:

DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

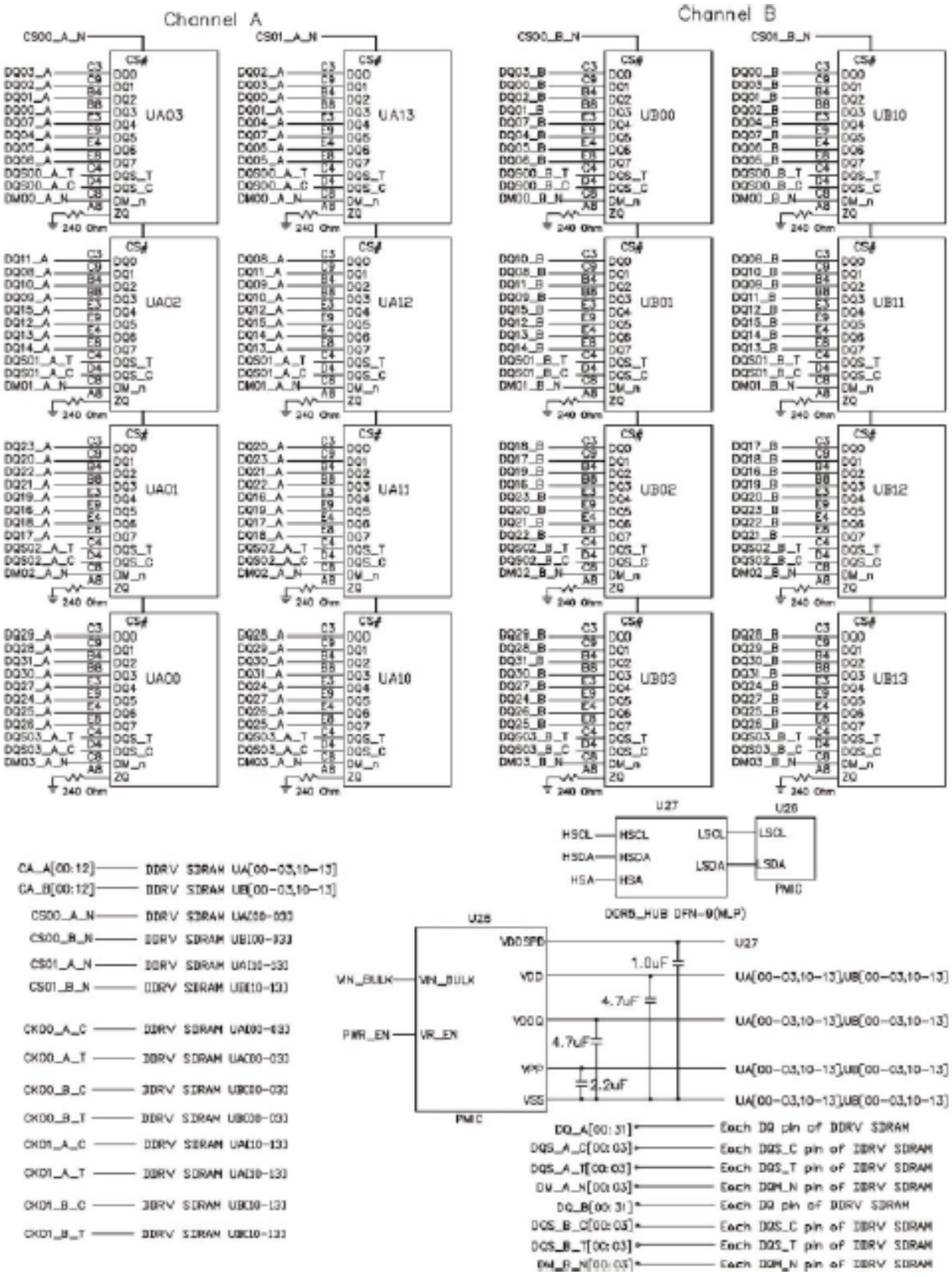
INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	I/O Levels	Description
CK[1:0]_A_t, CK[1:0]_B_t, CK[1:0]_A_c, CK[1:0]_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and con- trol input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:0]_A CA[12:0]_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
CS[1:0]_A_n CS[1:0]_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n pro- vides for external rank selection on systems with multiple ranks.
ALERT_n	Output	V_{DD}	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	V_{DD}	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.

Symbol	Type	I/O Levels	Description
PWR_GOOD	Input / Output	V_{DD}	Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropri- ate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresh- olds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input		Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input / Output		Host Sideband Bus Data:I2C/I3C-Basic data. When open drain, a pull-up resis- tor is required on the system motherboard.
HSA	Input		Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
DQ[31:0]_A DQ[31:0]_B	Input / Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB[3:0]_A CB[3:0]_B	Input / Output	VDD	DIMM ECC check bits. (Only applicable on ECC SODIMM or ECC UDIMM)

Symbol	Type	I/O Levels	Description
DQS[4:0]_A_t DQS[4:0]_B_t	Input / Output	VDD	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DQS[4:0]_A_c DQS[4:0]_B_c			
DM[3:0]_A_n DM[3:0]_B_n	Input	VDD	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM function is shared with TDQS on x8 devices. The function of DM_n is enabled by MR5:OP[5] = 1. Refer to Micron DDR5 component data sheet specification for further detail.
VIN_BULK	Supply		External Power Supply: 5V, 4.25V (min), 5.5V (max)
PWR_EN	Input		PMIC Enable: When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
VSS	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			No connect: No internal electrical connection is present.
NF			No function: May have internal connection present, but has no function.

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on VDD pin relative to Vss	V_{DD}	- 0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.3 ~ 1.4	V	1
Voltage on VPP pin relative to Vss	V_{PP}	- 0.3 ~ 2.1	V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.3 ~ 1.4	V	1
Storage temperature	TSTG	– 55 to +100	˚C	1,2

Notes:

1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

DRAM Component Operating Temperature Range

Symbol	Parameter	Temperature Range (Units : ℃)		Grade	Notes
		Min	Max		
Toper normal	Normal Operating Temperature	0	85	NT	1,2,3,4
Toper extended	Extended Operating Temperature	0	95	XT	1,2,3,4,5

Notes:

1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. All DDR5 SDRAMs are required to operate in NT and XT temperature ranges.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.

AC & DC OPERATING CONDITION

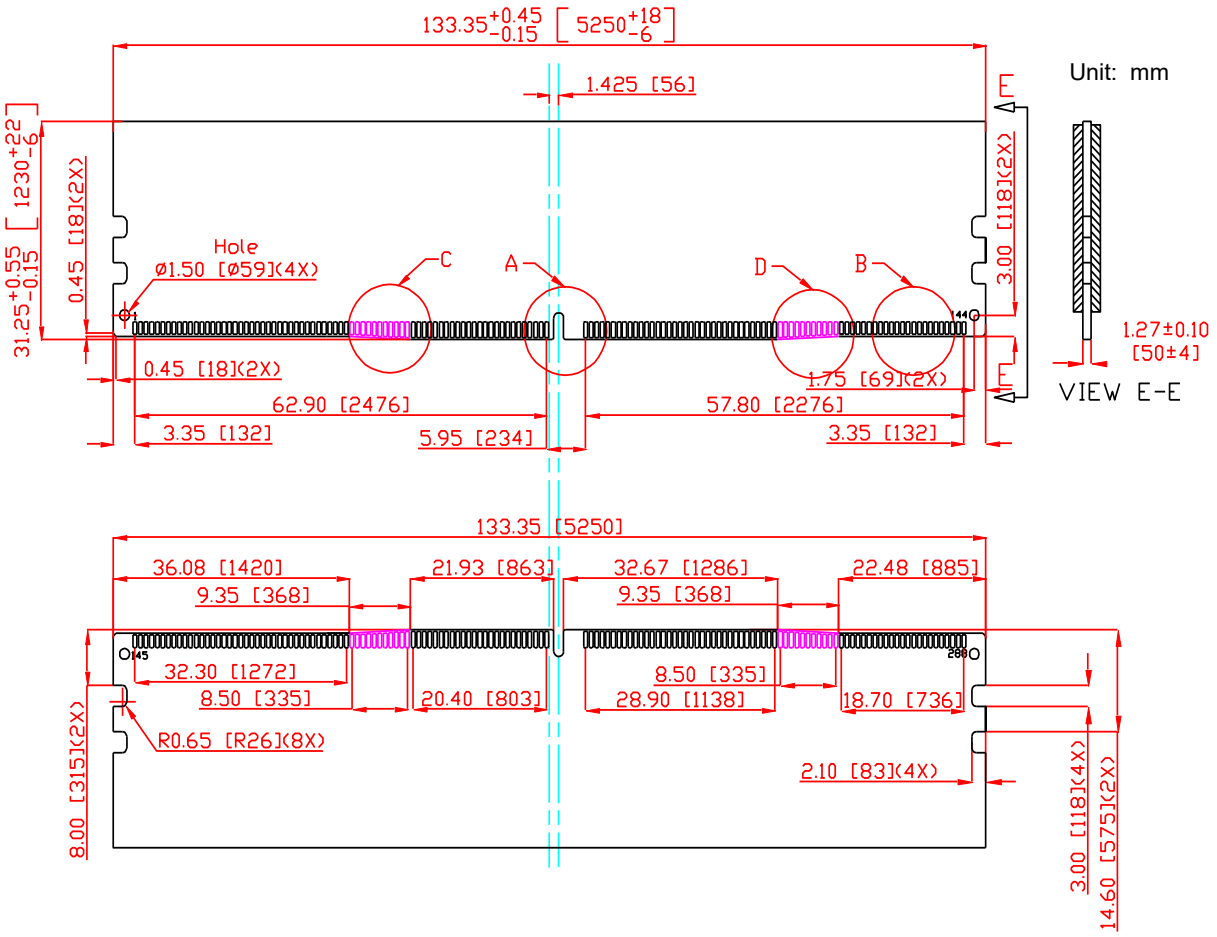
DIMM Voltage Requirements

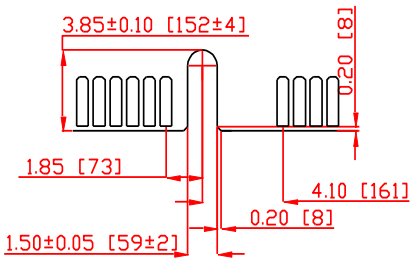
Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host Supply Voltage	4.25	5.0	5.5	2.A	Operational
SWA,SWB	PMIC Output Supply Voltage	-	1.1	-	Note 9	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	Note 9	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	Note 9	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025(maximum)	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020(maximum)	Operational

NOTE :

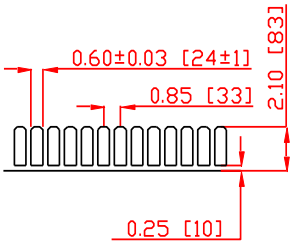
1. Input supplies referenced in this table are VIN_BULK and VIN.
2. During first power-on, the input voltage supply must reach a minimum of 4.25V for the PMIC to detect a valid input supply.
3. The ramp up rate is between 300mV and 4.0V.
4. The ramp down rate is between 4.0V and 300mV.
5. The area under the curve and above VIN_Bulk = TBD. The VIN_Bulk_AC spec must also be satisfied.
6. The minimum input current requirement is equal to the maximum output current on VOUT_1.8V and VOUT_1.0V LDO, plus the current required by the PMIC for its own use. The maximum input current is equal to the all VIN_Bulk input on the PMIC.
7. VIN_Bulk = 5.0V measured at room temperature. All circuitry, including output regulators and LDOs are off. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW
8. VIN_Bulk = 5.0V measured at room temperature. All output regulators and LDOs are on the 0A output load. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW.
9. Maximum and Minimum Current ratings depend on PMIC (5100)

Mechanical Drawing





Detail A



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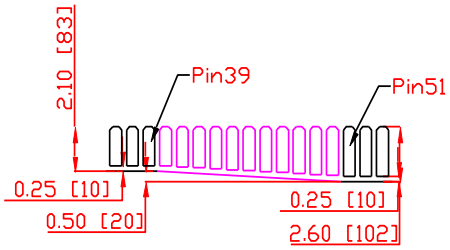

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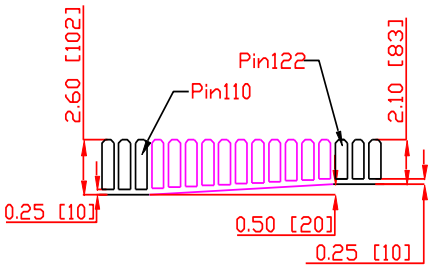

Detail D

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
1.0	4/12/2022	Initial release	
1.1	11/4/2022	Updated DIMM Voltage Requirements	
1.2	16/2/2024	Add Fully lead-free description	

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: +886-2-2267-8000
Fax: +886-2-2267-2261
amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9568
sa@apacerus.com

Japan

Apacer Technology Corp.
5F, Matsura Bldg., Shiba, Minato-Ku
Tokyo, 105-0014, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe

Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd.
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD , Shanghai , 200051, China
Tel: 86-21-6228-9939
Fax:86-21-6228-9936
sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd.
1874, South End C Cross,9th Block Jayanagar,
Bangalore-560069,INDIA.
Tel: 91-80-4152-9061/62
Fax: 91-80-4170-0215
sales_india@apacer.com