RoHS Compliant

8GB DDR5 SDRAM SO-DIMM

Halogen free

Product Specifications

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Version 1.1

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General Description

Apacer **D22.35491H.001** is a 8GB DDR5 SDRAM (Synchronous DRAM) SO-DIMM. This memory module consists of 4 pieces 1G x 16 bits DDR5 synchronous DRAMs in FBGA packages and 8K Bits EEPROM. The module is a 262-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Density	Speed	Organization	DRAM Composition	Rank
D22.35491H.001	8GB	5600 Mbps	1Gx64	1Gx16 *4	1

Key Parameters

Speed	DDR5-4800	DDR5-5600	Unit
	-CL40	-CL46	
tCK (min)	0.416	0.357	ns
CAS latency	40	46	nCK
tRCD (min)	16	16	ns
tRP (min)	16	16	ns
tRAS (min)	32	32	ns
tRC (min)	48	48	ns
CL-tRCD-tRP	40-39-39	46-45-45	nCK

Features:

- JEDEC standard compliant
- On-DIMM thermal sensor : Yes
- PCB: height 30 mm, lead pitch 0.5 mm (pin),
- VDD = VDDQ= 1.1V (1.067V to 1.166V)
- VPP = 1.8V (1.746V to 1.908V)、VDDSPD = 1.8V
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- CAS Latency (CL): 22,26,28,30,32,36,40,42,46,48,50
- CAS Write Latency (CWL): RL-2
- Operating temperature Tcase–(0℃~85℃)
- Average Refresh period 3.9us at lower than Tcase 85°C, 1.95us at 85°C < Tcase < 95 °C.
- All bank and same bank refresh
- Bi-Directional Differential Data Strobe
- 16-bit prefetch architecture
- On-die ECC
- ECC transparency and error scrub
- sPPR and hPPR capability
- Halogen free、Lead-free (RoHS compliant)

Pin Assignments

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
1	VIN_BULK	2	HSA	133	CK0_A_c	134	CK1_A_c
3	VIN_BULK	4	HSCL	135	VSS	136	VSS
5	RFU	6	HSDA	137	CK0_B_t	138	CK1_B_t
7	PWR_GOOD	8	PWR_EN	139	CK0_B_c	140	CK1_B_c
9	VSS	10	VSS	141	VSS	142	VSS
11	DQ0_A	12	DQ1_A	143	RFU	144	CA12_B
13	VSS	14	VSS	145	CA11_B	146	CA10_B
15	DQ2_A	16	DQ3_A	147	VSS	148	VSS
17	VSS	18	VSS	149	CA9_B	150	CA8_B
19	DM0_A_n	20	DQS0_A_c	151	CA7_B	152	CA6_B
21	VSS	22	DQS0_A_t	153	VSS	154	VSS
23	DQ4_A	24	VSS	155	CA5_B	156	CA4_B
25	VSS	26	DQ5_A	157	CA3_B	158	CA2_B
27	DQ6_A	28	VSS	159	VSS	160	VSS
29	VSS	30	DQ7_A	161	CS0_B_n	162	CA1_B
31	DQ8_A	32	VSS	163	RESET_n	164	CA0_B
33	VSS	34	DQ09_A	165	CS1_B_n	166	VSS
35	DQ10_A	36	VSS	167	VSS	168	CB0_B
37	VSS	38	DQ11_A	169	DQS4_B_c	170	VSS
39	DQS1_A_c	40	VSS	171	DQS4_B_t	172	CB1_B
41	DQS1_A_t	42	DM1_A_n	173	VSS	174	VSS
43	VSS	44	VSS	175	CB3_B	176	CB2_B
45	DQ12_A	46	DQ13_A	177	VSS	178	VSS
47	VSS	48	VSS	179	DQ0_B	180	DQ1_B
49	DQ14_A	50	DQ15_A	181	VSS	182	VSS
51	VSS	52	VSS	183	DQ2_B	184	DQ3_B
53	DQ16_A	54	DQ17_A	185	VSS	186	VSS
55	VSS	56	VSS	187	DM0_B_n	188	DQS0_B_c
57	DQ18_A	58	DQ19_A	189	VSS	190	DQS0_B_t
59	VSS	60	VSS	191	DQ4_B	192	VSS
61	DM2_A_n	62	DQS2_A_c	193	VSS	194	DQ5_B
63	VSS	64	DQS2_A_t	195	DQ6_B	196	VSS
65	DQ20_A	66	VSS	197	VSS	198	DQ7_B
67	VSS	68	DQ21_A	199	DQ8_B	200	VSS
69	DQ22_A	70	VSS	201	VSS	202	DQ9_B

Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
71	VSS	72	DQ23_A	203	DQ10_B	204	VSS
73	DQ24_A	74	VSS	205	VSS	206	DQ11_B
75	VSS	76	DQ25_A	207	DQS1_B_c	208	VSS
77	DQ26_A	78	VSS	209	DQS1_B_t	210	DM1_B_n
79	VSS	80	DQ27_A	211	VSS	212	VSS
81	DQS3_A_c	82	VSS	213	DQ12_B	214	DQ13_B
83	DQS3_A_t	84	DM3_A_n	215	VSS	216	VSS
85	VSS	86	VSS	217	DQ14_B	218	DQ15_B
87	DQ28_A	88	DQ29_A	219	VSS	220	VSS
89	VSS	90	VSS	221	DQ16_B	222	DQ17_B
91	DQ30_A	92	DQ31_A	223	VSS	224	VSS
93	VSS	94	VSS	225	DQ18_B	226	DQ19_B
95	CB0_A	96	CB1_A	227	VSS	228	VSS
97	VSS	98	VSS	229	DM2_B_n	230	DQS2_B_c
99	CB2_A	100	DQS4_A_c	231	VSS	232	DQS2_B_t
101	VSS	102	DQS4_A_t	233	DQ20_B	234	VSS
103	CB3_A	104	VSS	235	VSS	236	DQ21_B
105	VSS	106	CS0_A_n	237	DQ22_B	238	VSS
107	CA0_A	108	ALERT_n	239	VSS	240	DQ23_B
109	CA1_A	110	CS1_A_n	241	DQ24_B	242	VSS
111	VSS	112	VSS	243	VSS	244	DQ25_B
113	CA2_A	114	CA3_A	245	DQ26_B	246	VSS
115	CA4_A	116	CA5_A	247	VSS	248	DQ27_B
117	VSS	118	VSS	249	DQS3_B_c	250	VSS
119	CA6_A	120	CA7_A	251	DQS3_B_t	252	DM3_B_n
121	CA8_A	122	CA9_A	253	VSS	254	VSS
123	VSS	124	VSS	255	DQ28_B	256	DQ29_B
125	CA10_A	126	CA11_A	257	VSS	258	VSS
127	CA12_A	128	RFU	259	DQ30_B	260	DQ31_B
129	VSS	130	VSS	261	VSS	262	VSS
131	CK0_A_t	132	CK1_A_t	_	_	_	_

Pin Descriptions

Pin Name	Descripti
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits (Only applicable on ECC SODIMM or ECC UDIMM)
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)
HSCL	Side Band bus clock
HSDA	Side Band bus data
HSA	Side Band bus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a Known State
VIN_BULK	5 V power input supply to the PMIC for analog circuits
VSS	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

*Notes:

DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

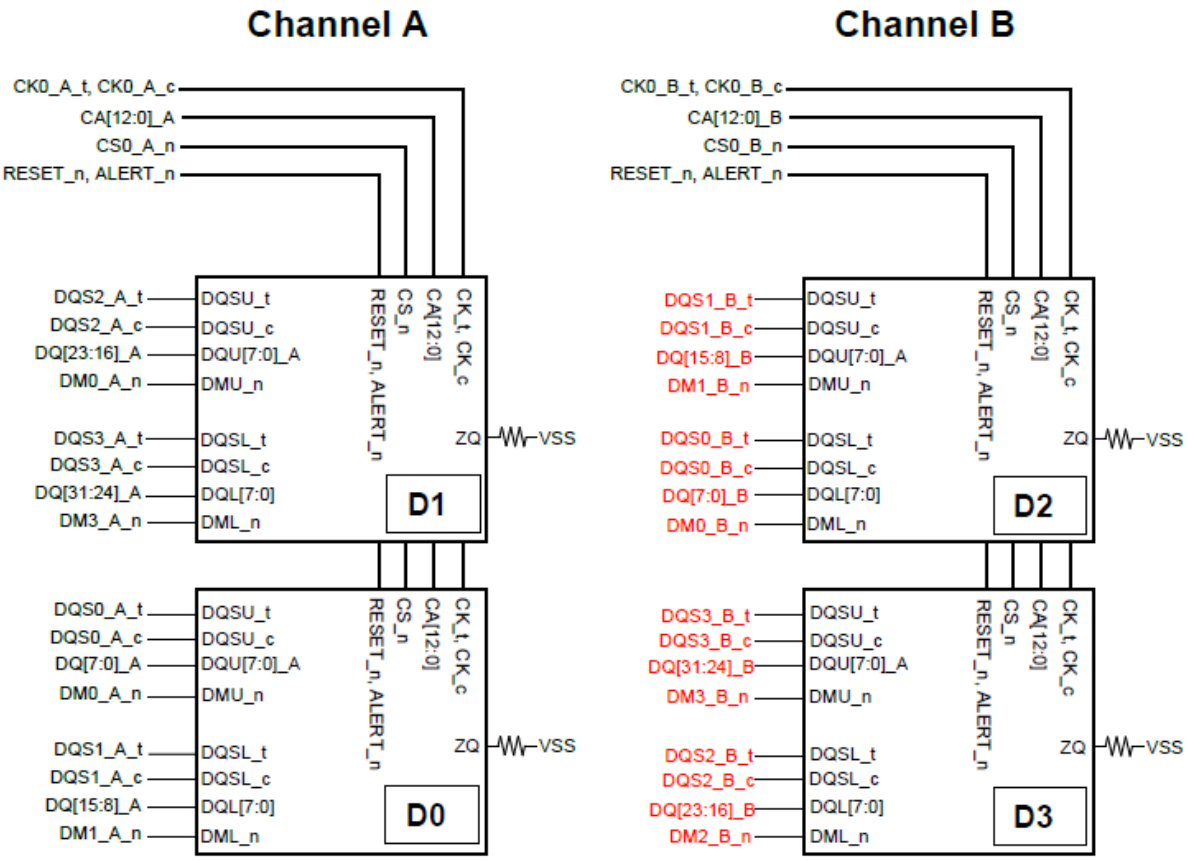
INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	I/O Levels	Description
CK[1:0]_A_t, CK[1:0]_B_t, CK[1:0]_A_c, CK[1:0]_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and con- trol input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:0]_A CA[12:0]_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
CS[1:0]_A_n CS[1:0]_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n pro- vides for external rank selection on systems with multiple ranks.
ALERT_n	Output	V_{DD}	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	V_{DD}	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.

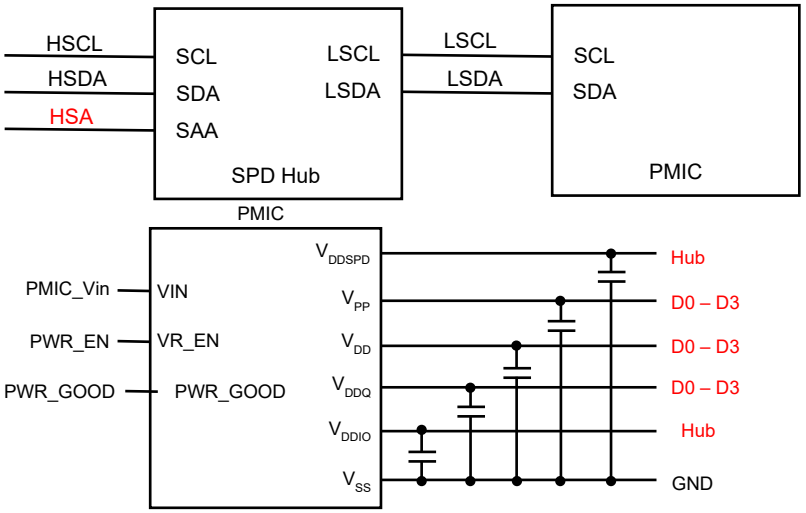
Symbol	Type	I/O Levels	Description
PWR_GOOD	Input / Output	V_{DD}	Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropri- ate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresh- olds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input		Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input / Output		Host Sideband Bus Data:I2C/I3C-Basic data. When open drain, a pull-up resis- tor is required on the system motherboard.
HSA	Input		Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
DQ[31:0]_A DQ[31:0]_B	Input / Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB[3:0]_A CB[3:0]_B	Input / Output	VDD	DIMM ECC check bits. (Only applicable on ECC SODIMM or ECC UDIMM)

Symbol	Type	I/O Levels	Description
DQS[4:0]_A_t DQS[4:0]_B_t	Input / Output	VDD	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DQS[4:0]_A_c DQS[4:0]_B_c			
DM[3:0]_A_n DM[3:0]_B_n	Input	VDD	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM function is shared with TDQS on x8 devices. The function of DM_n is enabled by MR5:OP[5] = 1. Refer to Micron DDR5 component data sheet specification for further detail.
VIN_BULK	Supply		External Power Supply: 5V, 4.25V (min), 5.5V (max)
PWR_EN	Input		PMIC Enable: When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
VSS	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			No connect: No internal electrical connection is present.
NF			No function: May have internal connection present, but has no function.

Functional Block Diagram



Note 1: Unless otherwise noted resistors are 15Ω ± 5%
Note 2: ZQ resistors are 240Ω ± 1%.
Note 3: CK1_[A:B]_t/c edge pin signals are each terminated with 33Ω ± 5% resistor to VSS.
Note 4: CS1_[A:B]_n edge pin signals are each terminated with 39Ω ± 5% resistor to VSS.



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on VDD pin relative to Vss	V_{DD}	- 0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.3 ~ 1.4	V	1
Voltage on VPP pin relative to Vss	V_{PP}	- 0.3 ~ 2.1	V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.3 ~ 1.4	V	1
Storage temperature	TSTG	– 55 to +100	˚C	1,2

Notes:

1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

DRAM Component Operating Temperature Range

Symbol	Parameter	Temperature Range (Units : ℃)		Grade	Notes
		Min	Max		
Toper normal	Normal Operating Temperature	0	85	NT	1,2,3,4
Toper extended	Extended Operating Temperature	0	95	XT	1,2,3,4,5

Notes:

1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. All DDR5 SDRAMs are required to operate in NT and XT temperature ranges.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.

AC & DC OPERATING CONDITION

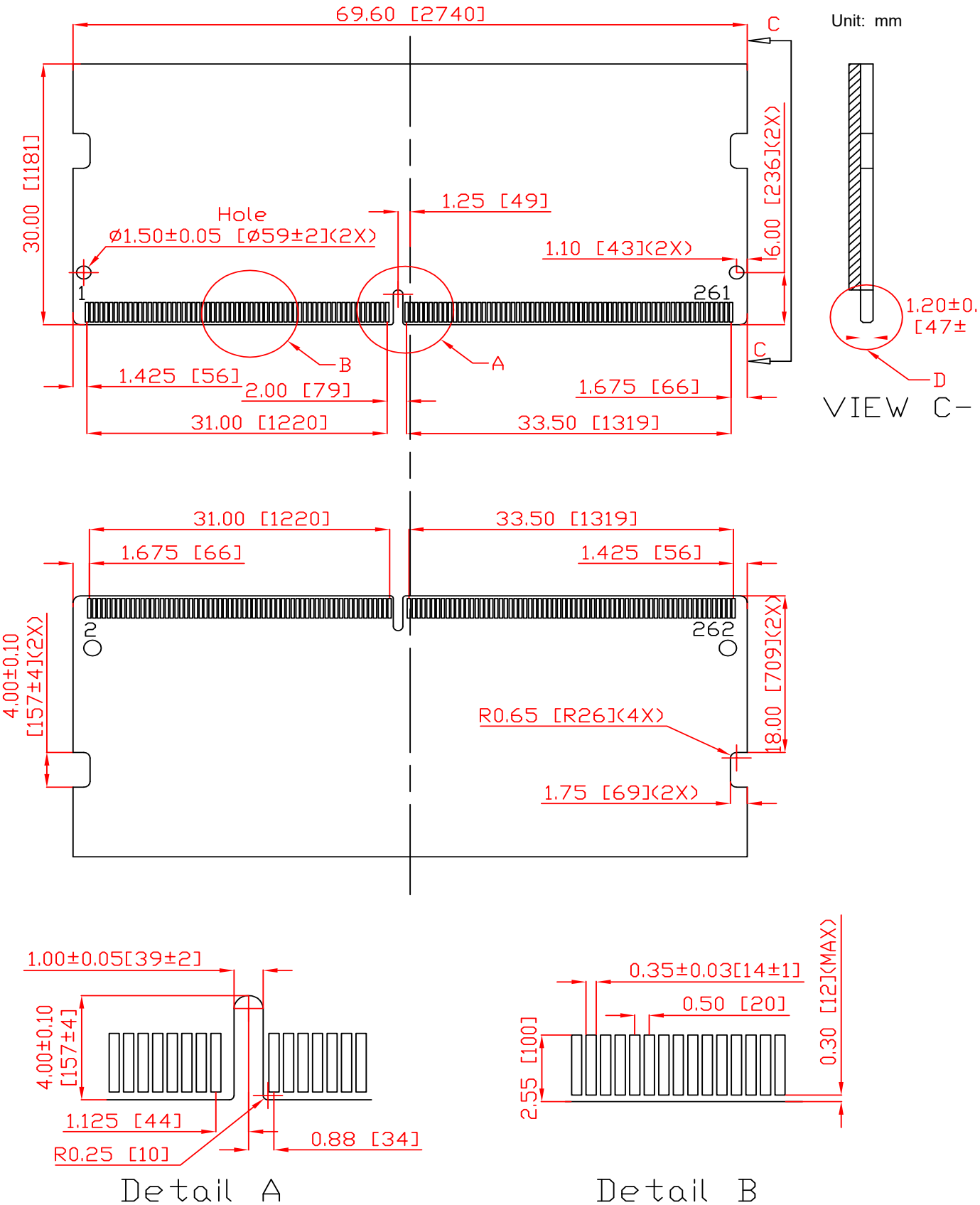
DIMM Voltage Requirements

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host Supply Voltage	4.25	5.0	5.5	2.A	Operational
SWA,SWB	PMIC Output Supply Voltage	-	1.1	-	Note 9	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	Note 9	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	Note 9	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025(maximum)	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020(maximum)	Operational

NOTE :

1. Input supplies referenced in this table are VIN_BULK and VIN.
2. During first power-on, the input voltage supply must reach a minimum of 4.25V for the PMIC to detect a valid input supply.
3. The ramp up rate is between 300mV and 4.0V.
4. The ramp down rate is between 4.0V and 300mV.
5. The area under the curve and above VIN_Bulk = TBD. The VIN_Bulk_AC spec must also be satisfied.
6. The minimum input current requirement is equal to the maximum output current on VOUT_1.8V and VOUT_1.0V LDO, plus the current required by the PMIC for its own use. The maximum input current is equal to the all VIN_Bulk input on the PMIC.
7. VIN_Bulk = 5.0V measured at room temperature. All circuitry, including output regulators and LDOs are off. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW
8. VIN_Bulk = 5.0V measured at room temperature. All output regulators and LDOs are on the 0A output load. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW.
9. Maximum and Minimum Current ratings depend on PMIC (5100)

Mechanical Drawing



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
1.0	4/12/2022	Initial release	
1.1	11/4/2022	Updated DIMM Voltage Requirements	

Global Presence

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