RoHS Compliant

4GB ECC DDR4 VLP Mini-UDIMM Halogen free

Product Specifications

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Version 0.4

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General Description

Apacer **D31.25180S.001** is a 512M x 72 DDR4 SDRAM (Synchronous DRAM) ECC DIMM. This high-density memory module consists of 9 pieces 512M x 8 bits DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
D31.25180S.001	12.8 GB/sec	1600 Mbps	800 MHz	CL11

Density	Organization	Component	Rank
4GB	512M x 72	512M x8*9	1

Key Parameters

MT/s	DDR4-1600	DDR4-1866	DDR4-2133	Unit
Grade	-CL11	-CL13	-CL15	
tCK (min)	1.25	1.07	0.93	ns
CAS latency	11	13	15	tCK
tRCD (min)	13.75	13.92	14.06	ns
tRP (min)	13.75	13.92	14.06	ns
tRAS (min)	35	34	33	ns
tRC (min)	48.75	47.92	47.05	ns
CL-tRCD-tRP	11-11-11	13-13-13	15-15-15	tCK

Specifications:

- Support ECC error detection and correction
- On-DIMM thermal sensor : Yes
- Organization: 512 words x 72 bits, 1 rank
- Integrating 9 pieces of 8G bits DDR4 SDRAM sealed FBGA
- Package: 288-pin socket type dual in-line memory module (Mini ECC DIMM)
- PCB: height 18.75 mm, lead pitch 0.5 mm (pin)
- Serial Presence Detect (SPD)
- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD = 2.2V to 3.6V
- 16 internal banks (4 Bank Groups)
- CAS Latency (CL): 6, 7, 8, 9, 10, 11
- CAS Write Latency (CWL): 5, 6, 7, 8
- Average refresh period

  7.8us at 0°C $\leqq$ TC $\leqq$ 85°C

  3.9us at 85°C $\leqq$ TC $\leqq$ 95°C
- Lead-free (RoHS compliant)
- Halogen free
- PCB: 30μ inch gold finger

Features:

- Functionality and operations comply with the DDR4 SDRAM datasheet
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	12V,NC	145	VREFCA	73	A1	217	RFU
2	12V,NC	146	SAVE_n,NC	74	VDD	218	VDD
3	RFU	147	RFU	75	CK0_t	219	CK1_t
4	VSS	148	VSS	76	CK0_c	220	CK1_c
5	DQ0	149	DQ4	77	VDD	221	VDD
6	VSS	150	VSS	78	RFU	222	RFU
7	DQ1	151	DQ5	79	VTT	223	VTT
8	VSS	152	VSS	KEY			
9	DQS0_c	153	TDQS9_t,DQS 9_t,DM0_n,DB I0_n	80	EVENT_n	224	PARITY
10	DQS0_t	154	TDQS9_c,DQS 9_c,NC	81	VDD	225	VDD
11	VSS	155	VSS	82	A0	226	BA1
12	DQ2	156	DQ6	83	BA0	227	A10/AP
13	VSS	157	VSS	84	VDD	228	VDD
14	DQ3	158	DQ7	85	RAS_n/A16	229	WE_n/A14
15	VSS	159	VSS	86	CS0_n	230	CAS_n/A15
16	DQ8	160	DQ12	87	VDD	231	VDD
17	VSS	161	VSS	88	ODT0	232	A13
18	DQ9	162	DQ13	89	CS1_n,NC	233	NC, A17
20	DQS1_c	164	TDQS10_t,DQS10_t,DM1_n, DBI1_n	91	ODT1,NC	235	NC,CS3_n,C1
21	DQS1_t	165	TDQS10_c,DQ S10_c,NC	92	C0,CS2_n,NC	236	NC,C2
22	VSS	166	VSS	93	VDD	237	VDD
23	DQ10	167	DQ14	94	RFU	238	RFU
24	VSS	168	VSS	95	VSS	239	VSS
25	DQ11	169	DQ15	96	DQ32	240	DQ36
26	VSS	170	VSS	97	VSS	241	VSS
27	DQ16	171	DQ20	98	DQ33	242	DQ37
28	VSS	172	VSS	99	VSS	243	VSS
29	DQ17	173	DQ21	100	DQS4_c	244	TDQS13_t,DQ S13_t,DM4_n, DBI4_n
30	VSS	174	VSS	101	DQS4_t	245	TDQS13_c,DQ S13_c,NC
31	DQS2_c	175	TDQS11_t,DQ S11_t,DM2_n, DBI2_n	102	VSS	246	VSS
32	DQS2_t	176	TDQS11_c,DQ S11_c,NC	103	DQ34	247	DQ38
33	VSS	177	VSS	104	VSS	248	VSS
34	DQ18	178	DQ22	105	DQ35	249	DQ39
35	VSS	179	VSS	106	VSS	250	VSS
36	DQ19	180	DQ23	107	DQ40	251	DQ44
37	VSS	181	VSS	108	VSS	252	VSS
38	DQ24	182	DQ28	109	DQ41	253	DQ45
39	VSS	183	VSS	110	VSS	254	VSS
40	DQ25	184	DQ29	111	DQS5_c	255	TDQS14_t,DQ S14_t,DM5_n, DBI5_n

41	VSS	185	VSS	112	DQS5_t	256	TDQS14_c,DQ S14_c,NC
42	DQS3_c	186	TDQS12_t,DQ S12_t,DM3_n, DBI3_n	113	VSS	257	VSS
43	DQS3_t	187	TDQS12_c,DQ S12_c,NC	114	DQ42	258	DQ46
44	VSS	188	VSS	115	VSS	259	VSS
45	DQ26	189	DQ30	116	DQ43	260	DQ47
46	VSS	190	VSS	117	VSS	261	VSS
47	DQ27	191	DQ31	118	DQ48	262	DQ52
48	VSS	192	VSS	119	VSS	263	VSS
49	CB0, NC	193	CB4, NC	120	DQ49	264	DQ53
50	VSS	194	VSS	121	VSS	265	VSS
51	CB1,NC	195	CB5, NC	122	DQS6_c	266	TDQS15_t,DQ S15_t,DM6_n, DBI6_n
52	VSS	196	VSS	123	DQS6_t	267	TDQS15_c,DQ S15_c,NC
53	DQS8_c	197	TDQS17_t,DQ S17_t,DM8_n, DBI8_n	124	VSS	268	VSS
54	DQS8_t	198	TDQS17_c,DQ S17_c,NC	125	DQ50	269	DQ54
55	VSS	199	VSS	126	VSS	270	VSS
56	CB2, NC	200	CB6, NC	127	DQ51	271	DQ55
57	VSS	201	VSS	128	VSS	272	VSS
58	CB3, NC	202	CB7, NC	129	DQ56	273	DQ60
59	VSS	203	VSS	130	VSS	274	VSS
60	ALERT_n	204	RESET_n	131	DQ57	275	DQ61
61	CKE0	205	RFU	132	VSS	276	VSS
62	VDD	206	VDD	133	DQS7_c	277	TDQS16_t,DQ S16_t,DM7_n, DBI7_n
63	ACT_n	207	CKE1, NC	134	DQS7_t	278	TDQS16_c,DQ S16_c,NC
64	BG0	208	BG1	135	VSS	279	VSS
65	VDD	209	VDD	136	DQ58	280	DQ62
66	A12/BC_n	210	A11	137	VSS	281	VSS
67	A9	211	A7	138	DQ59	282	DQ63
68	VDD	212	VDD	139	VSS	283	VSS
69	A8	213	A5	140	SA0	284	SA1
70	A6	214	A4	141	VDDSPD	285	SA2
71	VDD	215	VDD	142	SDA	286	SCL
72	A3	216	A2	143	VPP	287	VPP
				144	VPP	288	VPP

1. Light colored text indicates functions that are not applicable for RDIMM wiring. An example is the NC for pin 56 because RDIMMs defined by this specification will always have DIMM wiring for this pin.

*IC Component Composition :

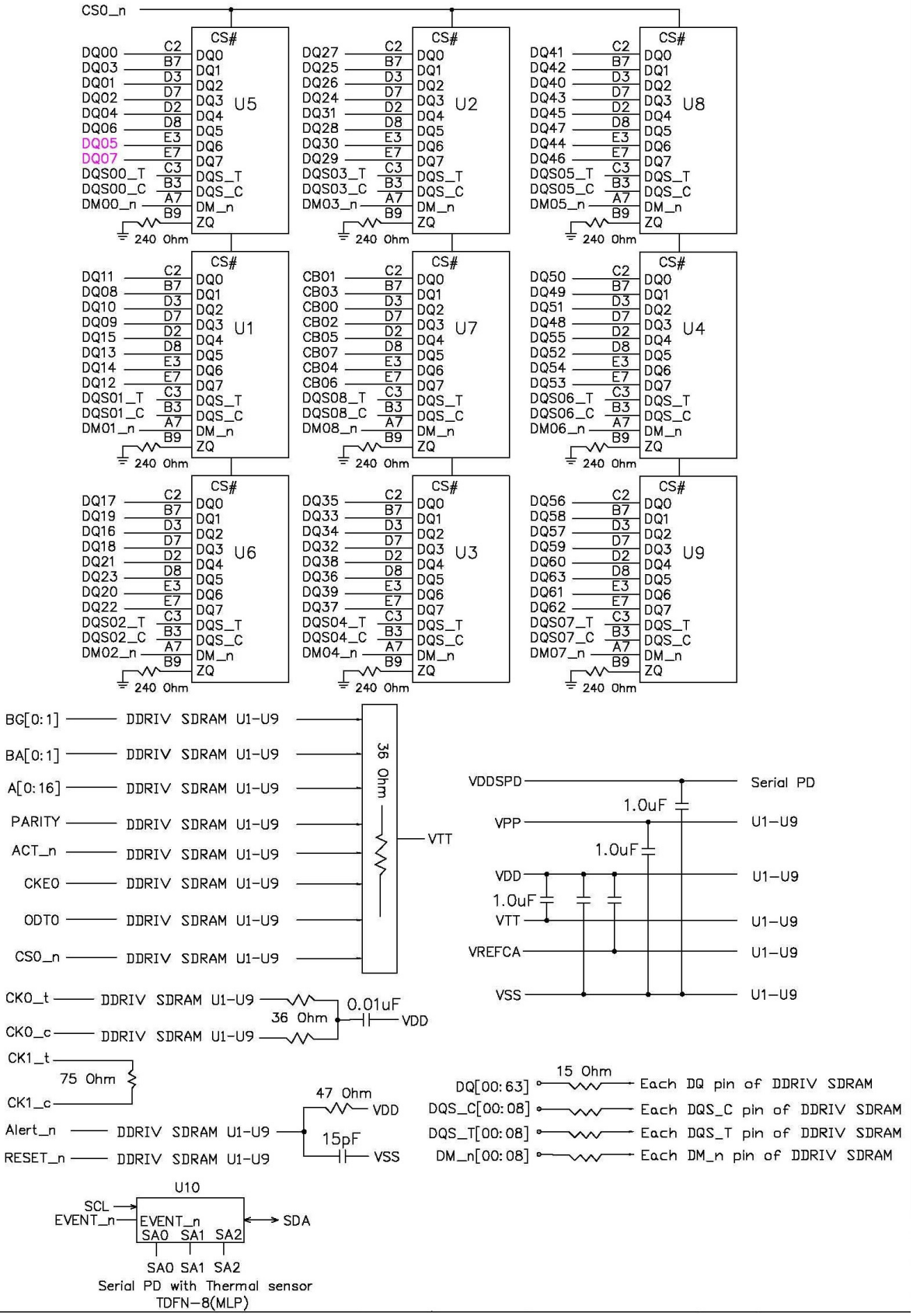
256Mx8	A0~A13		
512Mx8	A0~A14,	512Mx4	A0~A14
1024Mx8	A0~A15,	1024Mx4	A0~A15
2048Mx8	A0~A16,	2048Mx4	A0~A16

Pin Descriptions

Pin Name	Description
Ax[1*]	SDRAM address bus
BAx	SDRAM bank select
BGx	SDRAM bank group select
RAS_n[2*]	SDRAM row address strobe
CAS_n[3*]	SDRAM column address strobe
WE_n[4*]	SDRAM write enable
CSx_n	DIMM Rank Select Lines
CKEx	SDRAM clock enable lines
ODTx	SDRAM on-die termination control lines
ACT_n	SDRAM input for activate input
DQx	DIMM memory data bus
CBx	DIMM ECC check bits
TDQSx_t ; TDQSx_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs
DQSx_t	Data Buffer data strobes (positive line of differential pair)
DQSx_c	Data Buffer data strobes (negative line of differential pair)
DMx_n, DBIx_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)
CKx_t	SDRAM clock input (positive line of differential pair)
CKx_c	SDRAM clocks input (negative line of differential pair)
SCL	I^2C serial bus clock for SPD-TSE and register
SDA	I^2C serial bus data line for SPD-TSE and register
SAx	I^2C slave address select for SPD-TSE and register
PARITY	SDRAM parity input
VDD	SDRAM core power supply
12 V	Optional Power Supply on socket but not used on DIMM
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD-TSE positive power supply
ALERT_n	SDRAM ALERT_n output
VPP	SDRAM Supply
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

*Notes:
1. Address A17 is only valid for 16 Gb x4 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Description	Units	Notes
Voltage on VDD pin relative to Vss	V_{DD}	- 0.3 V ~ 1.5 V	V	1,2
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.3 V ~ 1.5 V	V	1,2
Voltage on VPP pin relative to Vss	V_{PP}	- 0.3 V ~ 3.0 V	V	3
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.3 V ~ 1.5 V	V	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
3. VPP must be equal or greater than VDD/VDDQ at all times

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	℃	1,2
	Extended Temperature Range	85 to 95	℃	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0℃ - 85℃ under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Activation Supply Voltage	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

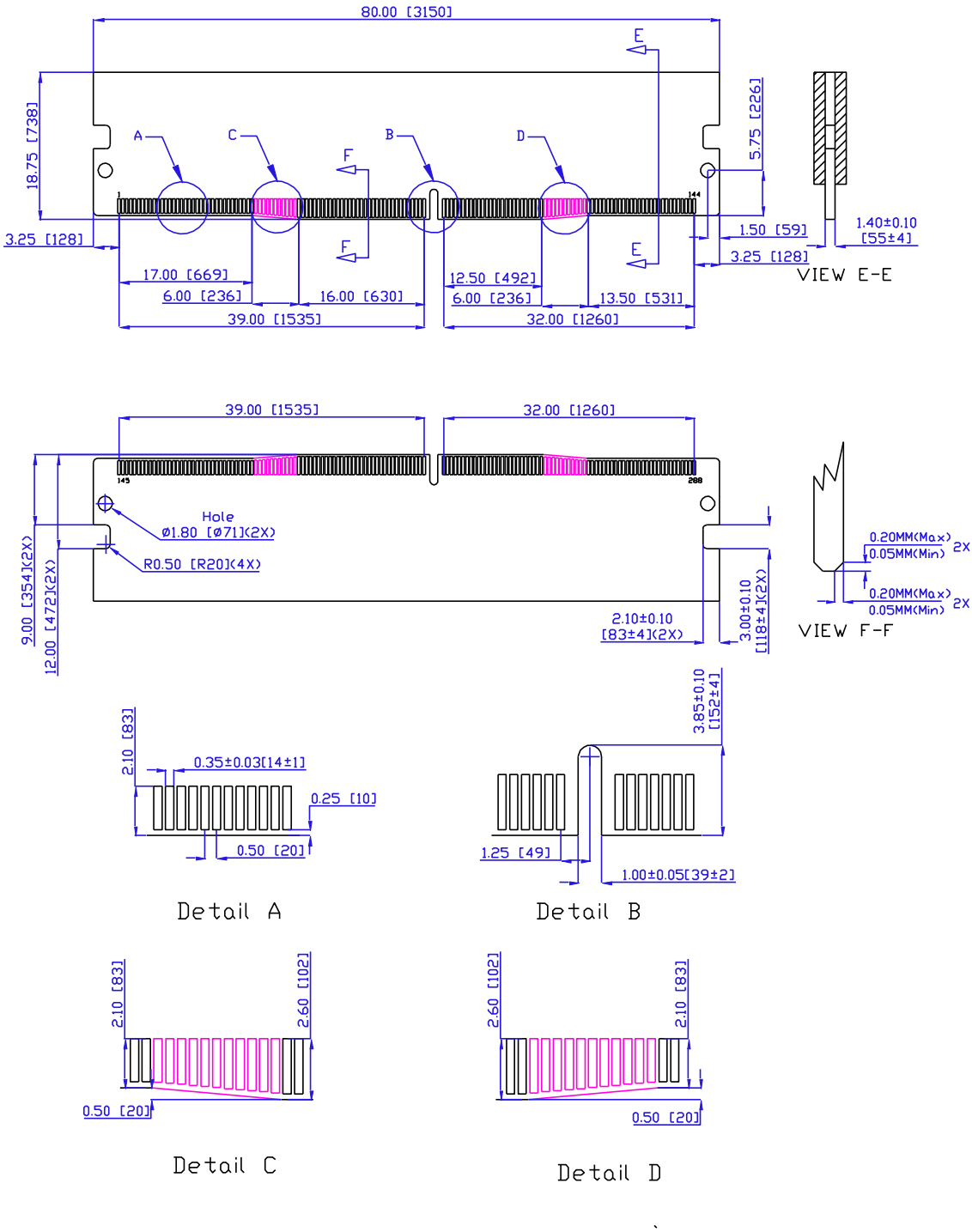
Environmental Requirements

Symbol	Parameter	Rating	Units	Notes
HOPR	Operating Humidity (relative)	10 to 90	%	
TSTG	Storage Temperature	-50 to +100	°C	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	kPa	1,2

Notes:

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

Mechanical Drawing



30μ inch gold finger

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.1	5/5/2014	Initial release	
0.2	11/2/2015	Updated VDDSPD	
0.3	03/15/2017	Add Environmental Requirements	
0.4	09/04/2017	Remove TOPR (Operating Temperature (ambient))	

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