

***RoHS Compliant***

**4GB DDR4 SDRAM SO-DIMM** Halogen free

***Product Specifications***

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**Version 0.2**



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## General Description

Apacer **78.B2GF0.AF00B** is a 512M x 64 DDR4 SDRAM (Synchronous DRAM) SO-DIMM. This high-density memory module consists of 8 pieces 512M x 8 bits with 4 banks DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 260-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

## Ordering Information

| Part Number    | Bandwidth | Speed Grade | Max Frequency | CAS Latency |
|----------------|-----------|-------------|---------------|-------------|
| 78.B2GF0.AF00B | 17 GB/sec | 2133 Mbps   | 1066 MHz      | CL15        |

| Density | Organization | Component | Rank |
|---------|--------------|-----------|------|
| 4GB     | 512M x 64    | 512M x8*8 | 1    |

## Key Parameters

| MT/s        | DDR4-1866 | DDR4-2133 | DDR4-2400 | Unit |
|-------------|-----------|-----------|-----------|------|
| Grade       | -CL13     | -CL15     | -CL17     |      |
| tCK (min)   | 1.07      | 0.93      | 0.83      | ns   |
| CAS latency | 13        | 15        | 17        | tCK  |
| tRCD (min)  | 13.92     | 14.06     | 14.16     | ns   |
| tRP (min)   | 13.92     | 14.06     | 14.16     | ns   |
| tRAS (min)  | 34        | 33        | 32        | ns   |
| tRC (min)   | 47.92     | 47.05     | 46.16     | ns   |
| CL-tRCD-tRP | 13-13-13  | 15-15-15  | 17-17-17  | tCK  |

## Specifications:

- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 512 words x 64 bits, 1 rank
- ◆ Integrating 8 pieces of 4G bits DDR4 SDRAM sealed FBGA
- ◆ Package: 260-pin socket type small outline dual in-line memory module (SO-DIMM)
- ◆ PCB: height 30.00 mm, lead pitch 0.50 mm (pin),
- ◆ Serial Presence Detect (SPD)
- ◆ Power Supply: VDD=1.2V (1.14V to 1.26V)
- ◆ VDDQ = 1.2V (1.14V to 1.26V)
- ◆ VPP = 2.5V (2.375V to 2.75V)
- ◆ VDDSPD = 2.2V to 3.6V
- ◆ 16 internal banks (4 Bank Groups)
- ◆ CAS Latency (CL): 10, 11, 12, 13, 14, 15
- ◆ CAS Write Latency (CWL): 9, 10, 11, 12, 14
- ◆ Average refresh period
  - 7.8us at  $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
  - 3.9us at  $85^{\circ}\text{C} \leq \text{TC} \leq 95^{\circ}\text{C}$
- ◆ Lead-free (RoHS compliant)
- ◆ Halogen free

## Features:

- ◆ Functionality and operations comply with the DDR4 SDRAM datasheet
- ◆ Bank Grouping is applied, and CAS to CAS latency (tCCD\_L, tCCD\_S) for the banks in the same or different bank group accesses are available
- ◆ Bi-Directional Differential Data Strobe
- ◆ 8 bit pre-fetch
- ◆ Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- ◆ Supports ECC error correction and detection
- ◆ Per DRAM Addressability is supported
- ◆ Internal Vref DQ level generation is available
- ◆ Write CRC is supported at all speed grades
- ◆ DBI (Data Bus Inversion) is supported(x8)
- ◆ CA parity (Command/Address Parity) mode is supported

## Pin Assignments

| Pin No. | Pin name-Front | Pin No. | Pin name-Back | Pin No. | Pin name-Front | Pin No. | Pin name-Back |
|---------|----------------|---------|---------------|---------|----------------|---------|---------------|
| 1       | VSS            | 2       | VSS           | 133     | A1             | 134     | EVENT_n       |
| 3       | DQ5            | 4       | DQ4           | 135     | VDD            | 136     | VDD           |
| 5       | VSS            | 6       | VSS           | 137     | CK0_t          | 138     | CK1_t         |
| 7       | DQ1            | 8       | DQ0           | 139     | CK0_c          | 140     | CK1_c         |
| 9       | VSS            | 10      | VSS           | 141     | VDD            | 142     | VDD           |
| 11      | DQS0_c         | 12      | DM0_n, DBI0_n | 143     | PARITY         | 144     | A0            |
| 13      | DQS0_t         | 14      | VSS           | 145     | BA1            | 146     | A10/AP        |
| 15      | VSS            | 16      | DQ6           | 147     | VDD            | 148     | VDD           |
| 17      | DQ7            | 18      | VSS           | 149     | CS0_n          | 150     | BA0           |
| 19      | VSS            | 20      | DQ2           | 151     | A14/WE_n       | 152     | A16/RAS_n     |
| 21      | DQ3            | 22      | VSS           | 153     | VDD            | 154     | VDD           |
| 23      | VSS            | 24      | DQ12          | 155     | ODT0           | 156     | A15/CAS_n     |
| 25      | DQ13           | 26      | VSS           | 157     | CS1_n          | 158     | A13           |
| 27      | VSS            | 28      | DQ8           | 159     | VDD            | 160     | VDD           |
| 29      | DQ9            | 30      | VSS           | 161     | ODT1           | 162     | C0, CS2_n, NC |
| 31      | VSS            | 32      | DQS1_c        | 163     | VDD            | 164     | VREFCA        |
| 33      | DM1_n, DBI1_n  | 34      | DQS1_t        | 165     | C1, CS3_n, NC  | 166     | SA2           |
| 35      | VSS            | 36      | VSS           | 167     | VSS            | 168     | VSS           |
| 37      | DQ15           | 38      | DQ14          | 169     | DQ37           | 170     | DQ36          |
| 39      | VSS            | 40      | VSS           | 171     | VSS            | 172     | VSS           |
| 41      | DQ10           | 42      | DQ11          | 173     | DQ33           | 174     | DQ32          |
| 43      | VSS            | 44      | VSS           | 175     | VSS            | 176     | VSS           |
| 45      | DQ21           | 46      | DQ20          | 177     | DQS4_c         | 178     | DM4_n, DBI4_n |
| 47      | VSS            | 48      | VSS           | 179     | DQS4_t         | 180     | VSS           |
| 49      | DQ17           | 50      | DQ16          | 181     | VSS            | 182     | DQ39          |
| 51      | VSS            | 52      | VSS           | 183     | DQ38           | 184     | VSS           |
| 53      | DQS2_c         | 54      | DM2_n, DBI2_n | 185     | VSS            | 186     | DQ35          |
| 55      | DQS2_t         | 56      | VSS           | 187     | DQ34           | 188     | VSS           |
| 57      | VSS            | 58      | DQ22          | 189     | VSS            | 190     | DQ45          |
| 59      | DQ23           | 60      | VSS           | 191     | DQ44           | 192     | VSS           |
| 61      | VSS            | 62      | DQ18          | 193     | VSS            | 194     | DQ41          |
| 63      | DQ19           | 64      | VSS           | 195     | DQ40           | 196     | VSS           |
| 65      | VSS            | 66      | DQ28          | 197     | VSS            | 198     | DQS5_c        |
| 67      | DQ29           | 68      | VSS           | 199     | DM5_n, DBI5_n  | 200     | DQS5_t        |
| 69      | VSS            | 70      | DQ24          | 201     | VSS            | 202     | VSS           |

| Pin No. | Pin name-Front | Pin No. | Pin name-Back | Pin No. | Pin name-Front | Pin No. | Pin name-Back |
|---------|----------------|---------|---------------|---------|----------------|---------|---------------|
| 71      | DQ25           | 72      | VSS           | 203     | DQ46           | 204     | DQ47          |
| 73      | VSS            | 74      | DQS3_c        | 205     | VSS            | 206     | VSS           |
| 75      | DM3_n, DBI3_n  | 76      | DQS3_t        | 207     | DQ42           | 208     | DQ43          |
| 77      | VSS            | 78      | VSS           | 209     | VSS            | 210     | VSS           |
| 79      | DQ30           | 80      | DQ31          | 211     | DQ52           | 212     | DQ53          |
| 81      | VSS            | 82      | VSS           | 213     | VSS            | 214     | VSS           |
| 83      | DQ26           | 84      | DQ27          | 215     | DQ49           | 216     | DQ48          |
| 85      | VSS            | 86      | VSS           | 217     | VSS            | 218     | VSS           |
| 87      | CB5, NC        | 88      | CB4, NC       | 219     | DQS6_c         | 220     | DM6_n, DBI6_n |
| 89      | VSS            | 90      | VSS           | 221     | DQS6_t         | 222     | VSS           |
| 91      | CB1, NC        | 92      | CB0, NC       | 223     | VSS            | 224     | DQ54          |
| 93      | VSS            | 94      | VSS           | 225     | DQ55           | 226     | VSS           |
| 95      | DQS8_c         | 96      | DM8_n, DBI8_n | 227     | VSS            | 228     | DQ50          |
| 97      | DQS8_t         | 98      | VSS           | 229     | DQ51           | 230     | VSS           |
| 99      | VSS            | 100     | CB6, NC       | 231     | VSS            | 232     | DQ60          |
| 101     | CB2, NC        | 102     | VSS           | 233     | DQ61           | 234     | VSS           |
| 103     | VSS            | 104     | CB7, NC       | 235     | VSS            | 236     | DQ57          |
| 105     | CB3, NC        | 106     | VSS           | 237     | DQ56           | 238     | VSS           |
| 107     | VSS            | 108     | RESET_n       | 239     | VSS            | 240     | DQS7_c        |
| 109     | CKE0           | 110     | CKE1          | 241     | DM7_n, DBI7_n  | 242     | DQS7_t        |
| 111     | VDD            | 112     | VDD           | 243     | VSS            | 244     | VSS           |
| 113     | BG1            | 114     | ACT_n         | 245     | DQ62           | 246     | DQ63          |
| 115     | BG0            | 116     | ALERT_n       | 247     | VSS            | 248     | VSS           |
| 117     | VDD            | 118     | VDD           | 249     | DQ58           | 250     | DQ59          |
| 119     | A12            | 120     | A11           | 251     | VSS            | 252     | VSS           |
| 121     | A9             | 122     | A7            | 253     | SCL            | 254     | SDA           |
| 123     | VDD            | 124     | VDD           | 255     | VDDSPD         | 256     | SA0           |
| 125     | A8             | 126     | A5            | 257     | VPP            | 258     | VTT           |
| 127     | A6             | 128     | A4            | 259     | VPP            | 260     | SA1           |
| 129     | VDD            | 130     | VDD           | —       | —              | —       | —             |
| 131     | A3             | 132     | A2            | —       | —              | —       | —             |

\*IC Component Composition :

|         |         |         |        |
|---------|---------|---------|--------|
| 256Mx8  | A0~A13  | 512Mx4  | A0~A14 |
| 512Mx8  | A0~A14, | 1024Mx4 | A0~A15 |
| 1024Mx8 | A0~A15, | 2048Mx4 | A0~A16 |
| 2048Mx8 | A0~A16, |         |        |

## Pin Descriptions

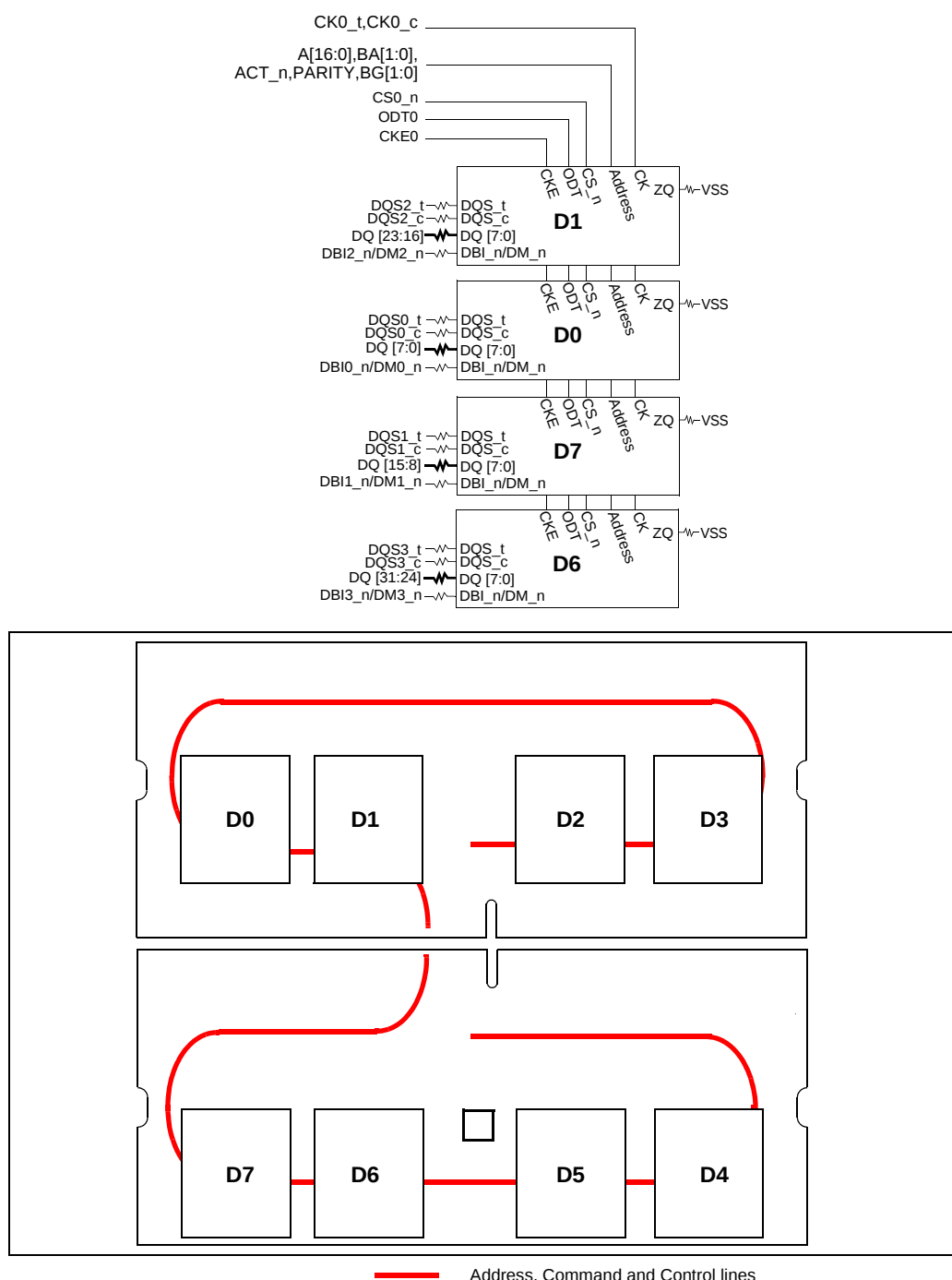
| Pin Name            | Description                                                                           |
|---------------------|---------------------------------------------------------------------------------------|
| AX <sup>1*</sup>    | SDRAM address bus                                                                     |
| BAx                 | SDRAM bank select                                                                     |
| BGx                 | SDRAM bank group select                                                               |
| RAS_n <sup>2*</sup> | SDRAM row address strobe                                                              |
| CAS_n <sup>3*</sup> | SDRAM column address strobe                                                           |
| WE_n <sup>4*</sup>  | SDRAM write enable                                                                    |
| CSx_n               | DIMM Rank Select Lines                                                                |
| CKEx                | SDRAM clock enable lines                                                              |
| ODTx                | SDRAM on-die termination control lines                                                |
| ACT_n               | SDRAM input for activate input                                                        |
| DQx                 | DIMM memory data bus                                                                  |
| CBx                 | DIMM ECC check bits                                                                   |
| TDQSx_t ; TDQSx_c   | Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs |
| DQSx_t              | Data Buffer data strobes (positive line of differential pair)                         |
| DQSx_c              | Data Buffer data strobes (negative line of differential pair)                         |
| DMx_n,<br>DBlx_n    | SDRAM data masks/data bus inversion(x8-based x72 DIMMs)                               |
| CKx_t               | SDRAM clock input (positive line of differential pair)                                |
| CKx_c               | SDRAM clocks input (negative line of differential pair)                               |
| SCL                 | I <sup>2</sup> C serial bus clock for SPD-TSE and register                            |
| SDA                 | I <sup>2</sup> C serial bus data line for SPD-TSE and register                        |
| SAX                 | I <sup>2</sup> C slave address select for SPD-TSE and register                        |
| PARITY              | SDRAM parity input                                                                    |
| VDD                 | SDRAM core power supply                                                               |
| 12 V                | Optional Power Supply on socket but not used on DIMM                                  |
| VREFCA              | SDRAM command/address reference supply                                                |
| VSS                 | Power supply return (ground)                                                          |
| VDDSPD              | Serial SPD-TSE positive power supply                                                  |
| ALERT_n             | SDRAM ALERT_n output                                                                  |
| VPP                 | SDRAM Supply                                                                          |
| RESET_n             | Set Register and SDRAMs to a Known State                                              |
| EVENT_n             | SPD signals a thermal event has occurred                                              |
| VTT                 | SDRAM I/O termination supply                                                          |
| RFU                 | Reserved for future use                                                               |

\*Notes:

1. Address A17 is only valid for 16 Gb x4 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS\_n is a multiplexed function with A16.
3. CAS\_n is a multiplexed function with A15.
4. WE\_n is a multiplexed function with A14.

# Functional Block Diagram

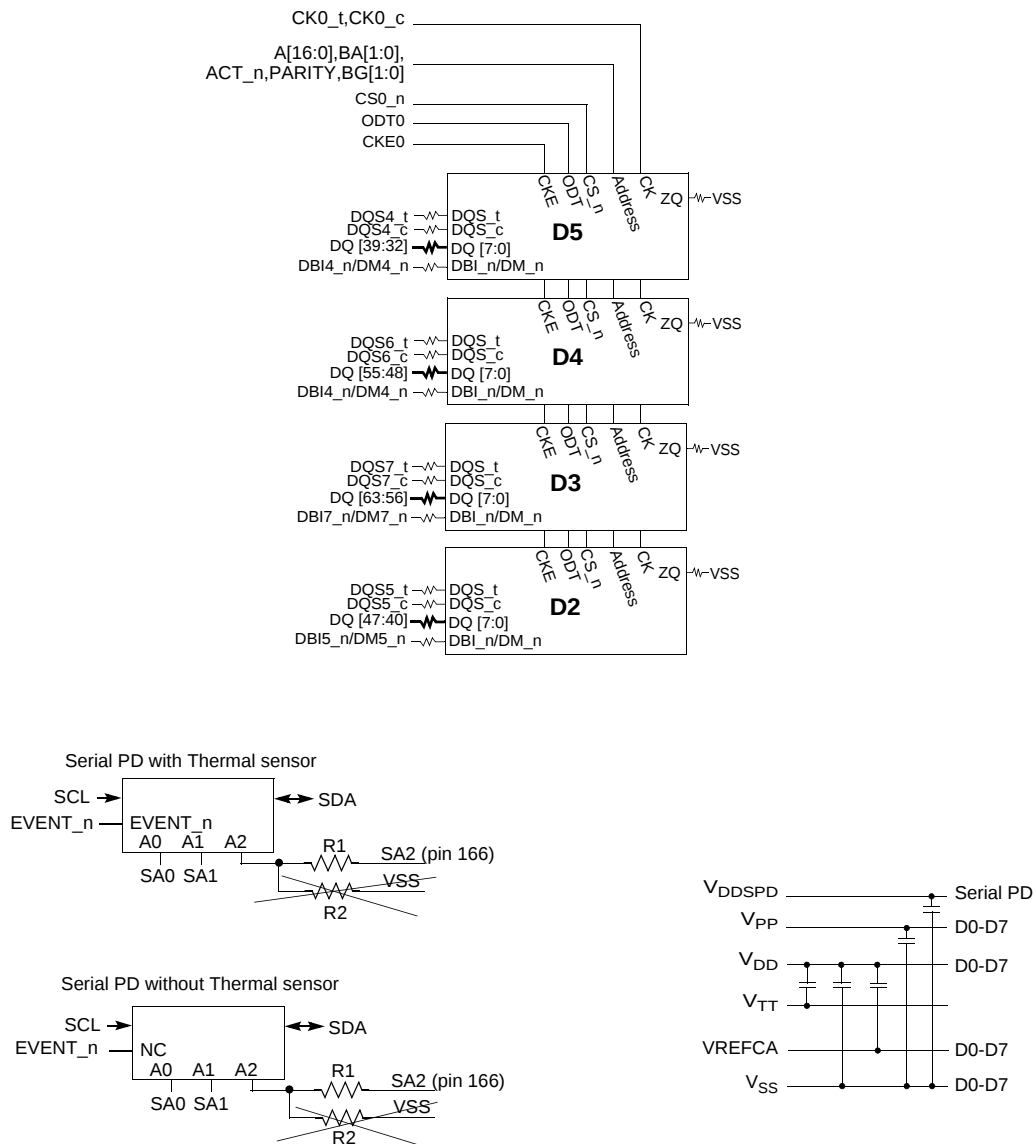
## Part 1 of 2



**Note 1:** Unless otherwise noted, resistor values are  $15 \Omega \pm 5\%$ .

**Note 2:** ZQ resistors are  $240 \Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.

## Part 2 of 2



**Note 1:** Unless otherwise noted, resistor values are  $15\ \Omega \pm 5\%$ .

**Note 2:** ZQ resistors are  $240\ \Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.

**Note 3:** To connect the SPD A2 input to the edge connector pin 166 install R1. SPD input A2 should not be tied to GND.

## Absolute Maximum Ratings

| Parameter                           | Symbol                             | Description     | Units | Notes |
|-------------------------------------|------------------------------------|-----------------|-------|-------|
| Voltage on VDD pin relative to Vss  | V <sub>DD</sub>                    | - 0.3 V ~ 1.5 V | V     | 1,3   |
| Voltage on VDDQ pin relative to Vss | V <sub>DDQ</sub>                   | - 0.3 V ~ 1.5 V | V     | 1,3   |
| Voltage on VPP pin relative to Vss  | V <sub>PP</sub>                    | - 0.3 V ~ 3.0 V | V     | 4     |
| Voltage on any pin relative to Vss  | V <sub>IN</sub> , V <sub>OUT</sub> | - 0.3 V ~ 3.0 V | V     | 1     |
| Storage Temperature                 | T <sub>STG</sub>                   | -55 to +100     | °C    | 1,2   |

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times

# DRAM Component Operating Temperature Range

| Symbol            | Parameter                          | Rating   | Units | Notes |
|-------------------|------------------------------------|----------|-------|-------|
| T <sub>OPER</sub> | Normal Operating Temperature Range | 0 to 85  | °C    | 1,2   |
|                   | Extended Temperature Range         | 85 to 95 | °C    | 1,3   |

## Notes:

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C - 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

## Operating Conditions

### Recommended DC Operating Conditions – DDR4 (1.2V) operation

| Symbol | Parameter                 | Rating |      |      | Units | Notes |
|--------|---------------------------|--------|------|------|-------|-------|
|        |                           | Min.   | Typ. | Max. |       |       |
| VDD    | Supply Voltage            | 1.14   | 1.2  | 1.26 | V     | 1,2,3 |
| VDDQ   | Supply Voltage for Output | 1.14   | 1.2  | 1.26 | V     | 1,2,3 |
| VPP    | Activation Supply Voltage | 2.375  | 2.5  | 2.75 | V     | 3     |

#### Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

## IDD Specifications

| Conditions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Symbol | HYNIX-M | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------|------|
| <b>Operating One Bank Active-Precharge Current (AL=0)</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> High between ACT and PRE; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,... ; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern   | IDD0   | 248     | mA   |
| <b>Operating One Bank Active-Precharge IPP Current</b><br><b>Same condition with IDD0</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | IPP0   | 21      | mA   |
| <b>Operating One Bank Active-Read-Precharge Current (AL=0)</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, nRCD, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> High between ACT, RD and PRE; <b>Command, Address, Bank Group Address, Bank Address Inputs, Data IO:</b> partially toggling; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,... ; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern | IDD1   | 328     | mA   |
| <b>Precharge Standby Current (AL=0)</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern                                                                                    | IDD2N  | 120     | mA   |
| <b>Precharge Standby ODT Current</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> VSSQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> toggling according ; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern                                                                               | IDD2NT | 144     | mA   |
| <b>Precharge Power-Down Current</b><br><b>CKE:</b> Low; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0                                                                                                                                                                          | IDD2P  | 88      | mA   |
| <b>Precharge Quiet Standby Current</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0                                                                                                                                                                      | IDD2Q  | 120     | mA   |
| <b>Active Standby Current</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern                                                                                                | IDD3N  | 216     | mA   |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |       |     |    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|----|
| <b>Active Standby IPP Current</b><br><b>Same condition with IDD3N</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IPP3N | 21  | mA |
| <b>Active Power-Down Current</b><br><b>CKE:</b> Low; <b>External clock:</b> On; <b>tCK, CL:</b> sRefer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0                                                                                                                                                                                                                                    | IDD3P | 160 | mA |
| <b>Operating Burst Read Current</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 82; <b>AL:</b> 0; <b>CS_n:</b> High between RD; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> seamless read data burst with different data between one burst and the next one according ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern | IDD4R | 808 | mA |
| <b>Operating Burst Write Current</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> High between WR; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> seamless write data burst with different data between one burst and the next one ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at HIGH; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern      | IDD4W | 848 | mA |
| <b>Burst Refresh Current (1X REF)</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL, nRFC:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n:</b> High between REF; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> REF command every nRFC ; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern                                                                                                                          | IDD5B | 960 | mA |
| <b>Burst Refresh Write IPP Current (1X REF)</b><br><b>Same condition with IDD5B</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | IPP5B | 174 | mA |
| <b>Self Refresh Current: Normal Temperature Range</b><br><b>TCASE:</b> 0 - 85°C; <b>Low Power Array Self Refresh (LP ASR) :</b> Normal4; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK_t</b> and <b>CK_c#:</b> LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> MID-LEVEL                                                                                                                                         | IDD6N | 88  | mA |
| <b>Self-Refresh Current: Extended Temperature Range</b><br><b>TCASE:</b> 0 - 95°C; <b>Low Power Array Self Refresh (LP ASR) :</b> Extended4; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK_t</b> and <b>CK_c:</b> LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Extended Temperature Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> MID-LEVEL                                                                                                                  | IDD6E | 112 | mA |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |       |      |    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|----|
| <b>Self-Refresh Current: Reduced Temperature Range</b><br><b>TCASE:</b> 0 - TBD (~35-45)°C; <b>Low Power Array Self Refresh (LP ASR)</b> : Reduced4; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK_t</b> and <b>CK_c#:</b> LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Extended Temperature Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> MID-LEVEL                                                                                                                                                        | IDD6R | 56   | mA |
| <b>Auto Self-Refresh Current</b><br><b>TCASE:</b> 0 - 95°C; <b>Low Power Array Self Refresh (LP ASR)</b> : Auto4; <b>Partial Array Self-Refresh (PASR):</b> Full Array; <b>CKE:</b> Low; <b>External clock:</b> Off; <b>CK_t</b> and <b>CK_c#:</b> LOW; <b>CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> 0; <b>CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:</b> High; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Auto Self-Refresh operation; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> MID-LEVEL                                                                                                                                                     | IDD6A | 120  | mA |
| <b>Operating Bank Interleave Read Current</b><br><b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:</b> Refer to Component Datasheet for detail pattern; <b>BL:</b> 81; <b>AL:</b> CL-1; <b>CS_n:</b> High between ACT and RDA; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling ; <b>Data IO:</b> read data bursts with different data between one burst and the next one ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> two times interleaved cycling through banks (0, 1, ...7) with different addressing; <b>Output Buffer and RTT:</b> Enabled in Mode Registers2; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> Refer to Component Datasheet for detail pattern | IDD7  | 1104 | mA |
| <b>Operating Bank Interleave Read IPP Current</b><br><b>Same condition with IDD7</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IPP7  | 90   | mA |
| <b>Maximum Power Down Current TBD</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IDD8  | 40   | mA |

Notes:

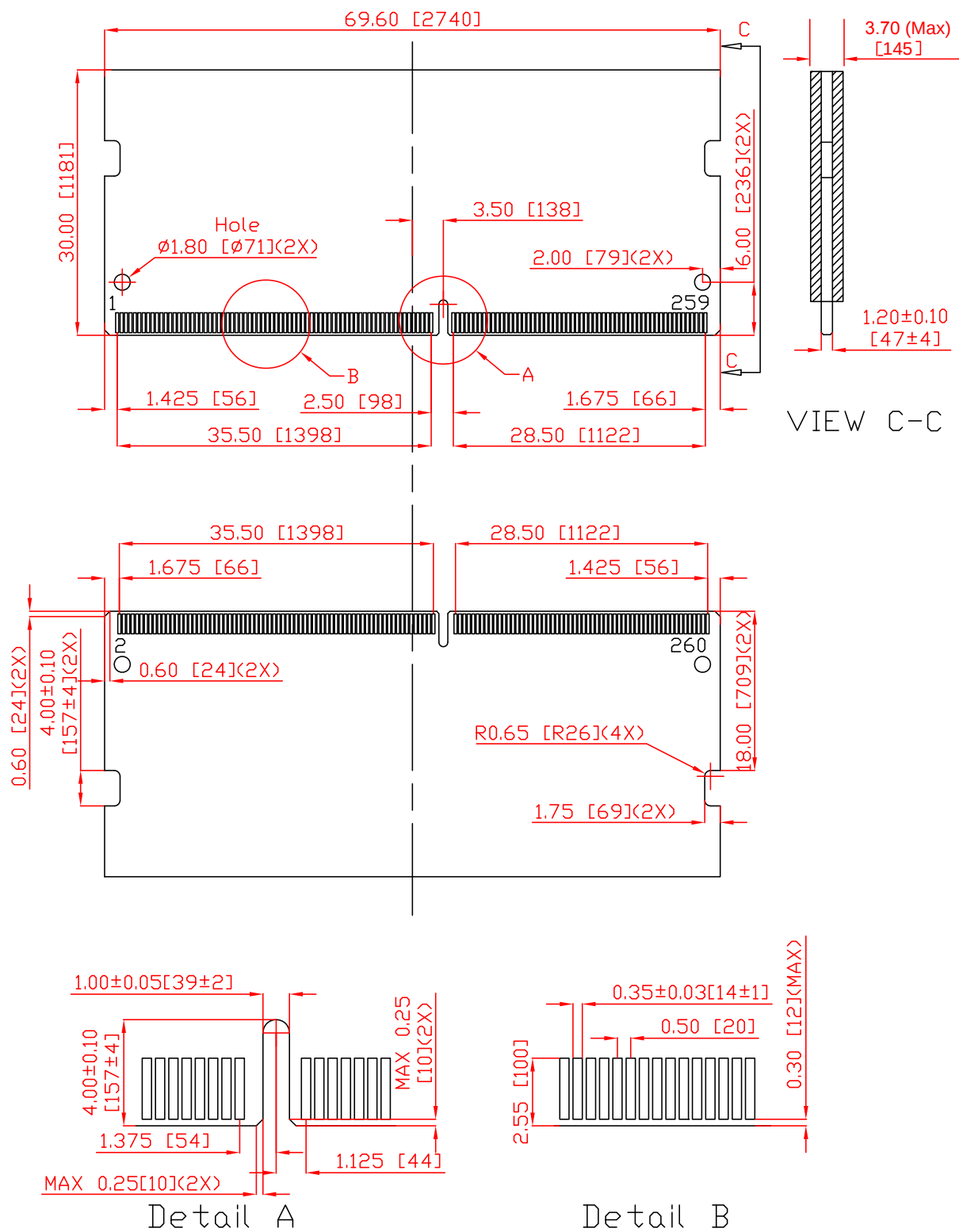
1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table 1.

[ Table1 ] DIMM Rank Status

| SEC DIMM | Operating Rank | The other Rank |
|----------|----------------|----------------|
| /DD0     | /DD0           | /DD2N          |
| /DD1     | /DD1           | /DD2N          |
| /DD2P    | IDD2P          | /DD2P          |
| /DD2N    | /DD2N          | /DD2N          |
| /DD2Q    | /DD2Q          | /DD2Q          |
| /DD3P    | /DD3P          | /DD3P          |
| /DD3N    | /DD3N          | /DD3N          |
| /DD4R    | /DD4R          | /DD2N          |
| /DD4W    | /DD4W          | /DD2N          |
| /DD5B    | /DD5B          | /DD2N          |
| /DD6     | /DD6           | /DD6           |
| /DD7     | /DD7           | /DD2N          |
| /DD8     | /DD8           | /DD8           |

# Mechanical Drawing

Unit: mm



(All dimensions are in millimeters with  $\pm 0.15$ mm tolerance unless specified otherwise.)

## Revision History

| Revision | Date      | Description     | Remark |
|----------|-----------|-----------------|--------|
| 0.1      | 5/5/2014  | Initial release |        |
| 0.2      | 11/2/2015 | Updated VDDSPD  |        |

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