RoHS Compliant

4GB DDR4 SDRAM SO-DIMM Halogen free

Product Specifications

November 4, 2015

Version 0.2

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General Description

Apacer **76.B355G.D040B** is a 512M x 64 DDR4 SDRAM (Synchronous DRAM) SO-DIMM. This high-density memory module consists of 8 pieces 512M x 8 bits with 4 banks DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 260-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
76.B355G.D040B	17 GB/sec	2133 Mbps	1066 MHz	CL15

Density	Organization	Component	Rank
4GB	512M x 64	512M x8*8	1

Key Parameters

MT/s	DDR4-1866	DDR4-2133	DDR4-2400	Unit
Grade	-CL13	-CL15	-CL17	
tCK (min)	1.07	0.93	0.83	ns
CAS latency	13	15	17	tCK
tRCD (min)	13.92	14.06	14.16	ns
tRP (min)	13.92	14.06	14.16	ns
tRAS (min)	34	33	32	ns
tRC (min)	47.92	47.05	46.16	ns
CL-tRCD-tRP	13-13-13	15-15-15	17-17-17	tCK

Specifications:

- On-DIMM thermal sensor : No
- Organization: 512 words x 64 bits, 1 rank
- Integrating 8 pieces of 4G bits DDR4 SDRAM sealed FBGA
- Package: 260-pin socket type small outline dual in-line memory module (SO-DIMM)
- PCB: height 30.00 mm, lead pitch 0.50 mm (pin),
- Serial Presence Detect (SPD)
- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD = 2.2V to 3.6V
- 16 internal banks (4 Bank Groups)
- CAS Latency (CL): 10, 11, 12, 13, 14, 15
- CAS Write Latency (CWL): 9, 10, 11,12,14
- Average refresh period
  7.8us at 0°C ≦ TC ≦ 85°C
  3.9us at 85°C ≦ TC ≦ 95°C
- Lead-free (RoHS compliant)
- Halogen free

Features:

- Functionality and operations comply with the DDR4 SDRAM datasheet
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

Pin Assignments

Pin No.	Pin name-Front	Pin No.	Pin name-Back	Pin No.	Pin name-Front	Pin No.	Pin name-Back
1	VSS	2	VSS	133	A1	134	EVENT_n
3	DQ5	4	DQ4	135	VDD	136	VDD
5	VSS	6	VSS	137	CK0_t	138	CK1_t
7	DQ1	8	DQ0	139	CK0_c	140	CK1_c
9	VSS	10	VSS	141	VDD	142	VDD
11	DQS0_c	12	DM0_n, DBI0_n	143	PARITY	144	A0
13	DQS0_t	14	VSS	145	BA1	146	A10/AP
15	VSS	16	DQ6	147	VDD	148	VDD
17	DQ7	18	VSS	149	CS0_n	150	BA0
19	VSS	20	DQ2	151	A14/WE_n	152	A16/RAS_n
21	DQ3	22	VSS	153	VDD	154	VDD
23	VSS	24	DQ12	155	ODT0	156	A15/CAS_n
25	DQ13	26	VSS	157	CS1_n	158	A13
27	VSS	28	DQ8	159	VDD	160	VDD
29	DQ9	30	VSS	161	ODT1	162	C0, CS2_n, NC
31	VSS	32	DQS1_c	163	VDD	164	VREFCA
33	DM1_n, DBI1_n	34	DQS1_t	165	C1, CS3_n, NC	166	SA2
35	VSS	36	VSS	167	VSS	168	VSS
37	DQ15	38	DQ14	169	DQ37	170	DQ36
39	VSS	40	VSS	171	VSS	172	VSS
41	DQ10	42	DQ11	173	DQ33	174	DQ32
43	VSS	44	VSS	175	VSS	176	VSS
45	DQ21	46	DQ20	177	DQS4_c	178	DM4_n, DBI4_n
47	VSS	48	VSS	179	DQS4_t	180	VSS
49	DQ17	50	DQ16	181	VSS	182	DQ39
51	VSS	52	VSS	183	DQ38	184	VSS
53	DQS2_c	54	DM2_n, DBI2_n	185	VSS	186	DQ35
55	DQS2_t	56	VSS	187	DQ34	188	VSS
57	VSS	58	DQ22	189	VSS	190	DQ45
59	DQ23	60	VSS	191	DQ44	192	VSS
61	VSS	62	DQ18	193	VSS	194	DQ41
63	DQ19	64	VSS	195	DQ40	196	VSS
65	VSS	66	DQ28	197	VSS	198	DQS5_c
67	DQ29	68	VSS	199	DM5_n, DBI5_n	200	DQS5_t
69	VSS	70	DQ24	201	VSS	202	VSS

Pin No.	Pin name-Front	Pin No.	Pin name-Back	Pin No.	Pin name-Front	Pin No.	Pin name-Back
71	DQ25	72	VSS	203	DQ46	204	DQ47
73	VSS	74	DQS3_c	205	VSS	206	VSS
75	DM3_n, DBI3_n	76	DQS3_t	207	DQ42	208	DQ43
77	VSS	78	VSS	209	VSS	210	VSS
79	DQ30	80	DQ31	211	DQ52	212	DQ53
81	VSS	82	VSS	213	VSS	214	VSS
83	DQ26	84	DQ27	215	DQ49	216	DQ48
85	VSS	86	VSS	217	VSS	218	VSS
87	CB5, NC	88	CB4, NC	219	DQS6_c	220	DM6_n, DBI6_n
89	VSS	90	VSS	221	DQS6_t	222	VSS
91	CB1, NC	92	CB0, NC	223	VSS	224	DQ54
93	VSS	94	VSS	225	DQ55	226	VSS
95	DQS8_c	96	DM8_n, DBI8_n	227	VSS	228	DQ50
97	DQS8_t	98	VSS	229	DQ51	230	VSS
99	VSS	100	CB6, NC	231	VSS	232	DQ60
101	CB2, NC	102	VSS	233	DQ61	234	VSS
103	VSS	104	CB7, NC	235	VSS	236	DQ57
105	CB3, NC	106	VSS	237	DQ56	238	VSS
107	VSS	108	RESET_n	239	VSS	240	DQS7_c
109	CKE0	110	CKE1	241	DM7_n, DBI7_n	242	DQS7_t
111	VDD	112	VDD	243	VSS	244	VSS
113	BG1	114	ACT_n	245	DQ62	246	DQ63
115	BG0	116	ALERT_n	247	VSS	248	VSS
117	VDD	118	VDD	249	DQ58	250	DQ59
119	A12	120	A11	251	VSS	252	VSS
121	A9	122	A7	253	SCL	254	SDA
123	VDD	124	VDD	255	VDDSPD	256	SA0
125	A8	126	A5	257	VPP	258	VTT
127	A6	128	A4	259	VPP	260	SA1
129	VDD	130	VDD	–	–	–	–
131	A3	132	A2	–	–	–	–

*IC Component Composition :

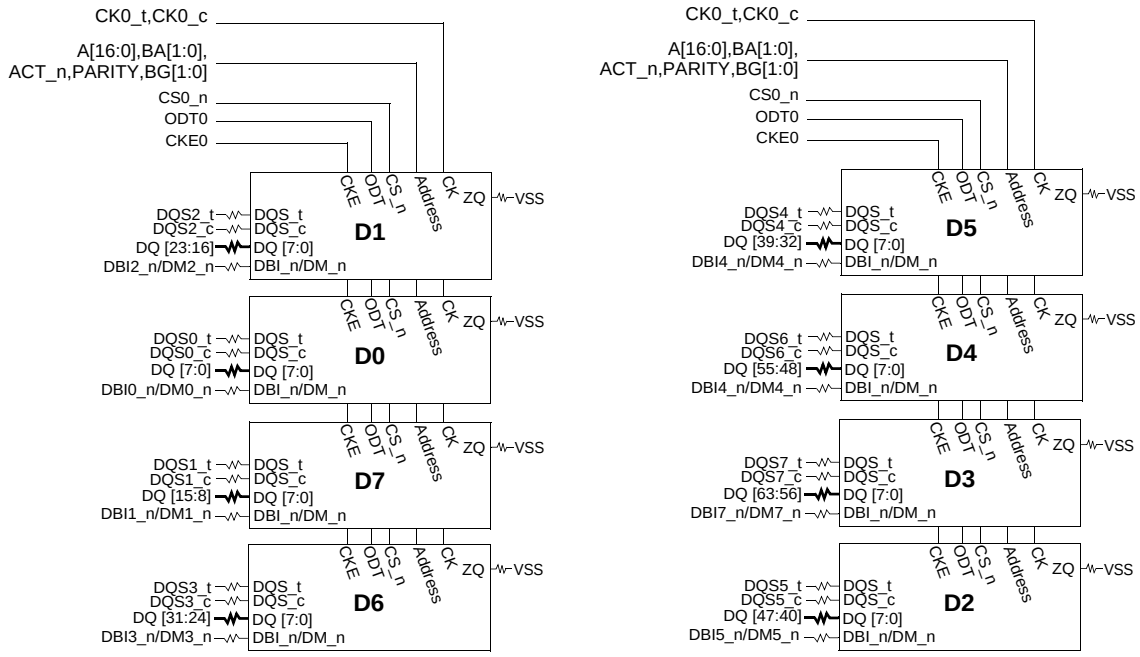
256Mx8	A0~A13		
512Mx8	A0~A14,	512Mx4	A0~A14
1024Mx8	A0~A15,	1024Mx4	A0~A15
2048Mx8	A0~A16,	2048Mx4	A0~A16

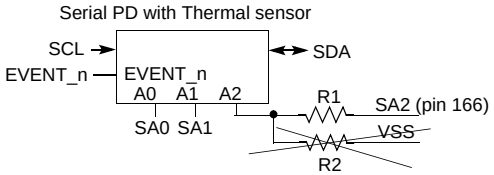
Pin Descriptions

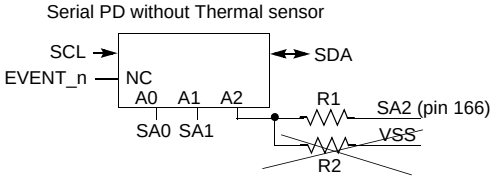
Pin Name	Description
Ax[1*]	SDRAM address bus
BAx	SDRAM bank select
BGx	SDRAM bank group select
RAS_n[2*]	SDRAM row address strobe
CAS_n[3*]	SDRAM column address strobe
WE_n[4*]	SDRAM write enable
CSx_n	DIMM Rank Select Lines
CKEx	SDRAM clock enable lines
ODTx	SDRAM on-die termination control lines
ACT_n	SDRAM input for activate input
DQx	DIMM memory data bus
CBx	DIMM ECC check bits
TDQSx_t ; TDQSx_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs
DQSx_t	Data Buffer data strobes (positive line of differential pair)
DQSx_c	Data Buffer data strobes (negative line of differential pair)
DMx_n, DBIx_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)
CKx_t	SDRAM clock input (positive line of differential pair)
CKx_c	SDRAM clocks input (negative line of differential pair)
SCL	I^2C serial bus clock for SPD-TSE and register
SDA	I^2C serial bus data line for SPD-TSE and register
SAx	I^2C slave address select for SPD-TSE and register
PARITY	SDRAM parity input
VDD	SDRAM core power supply
12 V	Optional Power Supply on socket but not used on DIMM
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD-TSE positive power supply
ALERT_n	SDRAM ALERT_n output
VPP	SDRAM Supply
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

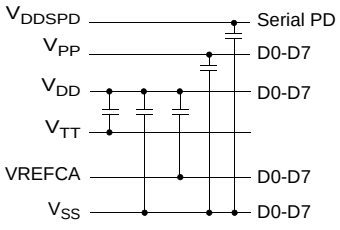
*Notes:
1. Address A17 is only valid for 16 Gb x4 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Functional Block Diagram









Note 1: Unless otherwise noted, resistor values are 15 Ω ± 5%.
Note 2: ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
Note 3: To connect the SPD A2 input to the edge connector pin 166 install R1. SPD input A2 should not be tied to GND.

Absolute Maximum Ratings

Parameter	Symbol	Description	Units	Notes
Voltage on VDD pin relative to Vss	V_{DD}	- 0.3 V ~ 1.5 V	V	1,3
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.3 V ~ 1.5 V	V	1,3
Voltage on VPP pin relative to Vss	V_{PP}	- 0.3 V ~ 3.0 V	V	4
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.3 V ~ 3.0 V	V	1
Storage Temperature	T_{STG}	-55 to +100	℃	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	℃	1,2
	Extended Temperature Range	85 to 95	℃	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0℃ - 85℃ under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Activation Supply Voltage	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

IDD Specifications

Conditions	Symbol	SAMSUNG-D	Unit
Operating One Bank Active-Precharge Current (AL=0) **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD0	270	mA
Operating One Bank Active-Precharge IPP Current **Same condition with IDD0**	IPP0	32	mA
Operating One Bank Active-Read-Precharge Current (AL=0) **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling; **DM_n:** sta-ble at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD1	350	mA
Precharge Standby Current (AL=0) **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD2N	130	mA
Precharge Standby ODT Current **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** toggling according ; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD2NT	150	mA
Precharge Power-Down Current **CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0	IDD2P	90	mA
Precharge Quiet Standby Current **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0	IDD2Q	120	mA
Active Standby Current **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:**Refer to Component Datasheet for detail pattern	IDD3N	240	mA

Active Standby IPP Current **Same condition with IDD3N**	IPP3N	24	mA
Active Power-Down Current **CKE:** Low; **External clock:** On; **tCK, CL**: sRefer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0	IDD3P	120	mA
Operating Burst Read Current **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 82; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless read data burst with different data between one burst and the next one according ; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD4R	760	mA
Operating Burst Write Current **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless write data burst with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at HIGH; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD4W	620	mA
Burst Refresh Current (1X REF) **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC ; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD5B	1230	mA
Burst Refresh Write IPP Current (1X REF) **Same condition with IDD5B**	IPP5B	120	mA
Self Refresh Current: Normal Temperature Range ***T*CASE:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal4; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** MID-LEVEL	IDD6N	100	mA
Self-Refresh Current: Extended Temperature Range ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended4; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** MID-LEVEL	IDD6E	130	mA

Self-Refresh Current: Reduced Temperature Range ***T*CASE:** 0 - TBD (~35-45)°C; **Low Power Array Self Refresh (LP ASR)** : Reduced4; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** MID-LEVEL	IDD6R	80	mA
Auto Self-Refresh Current ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto4;**Partial Array Self-Refresh (PASR)**: Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** MID-LEVEL	IDD6A	100	mA
Operating Bank Interleave Read Current **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: Refer to Component Datasheet for detail pattern; **BL:** 81; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** read data bursts with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern	IDD7	1180	mA
Operating Bank Interleave Read IPP Current **Same condition with IDD7**	IPP7	60	mA
Maximum Power Down Current TBD	IDD8	60	mA

Notes:

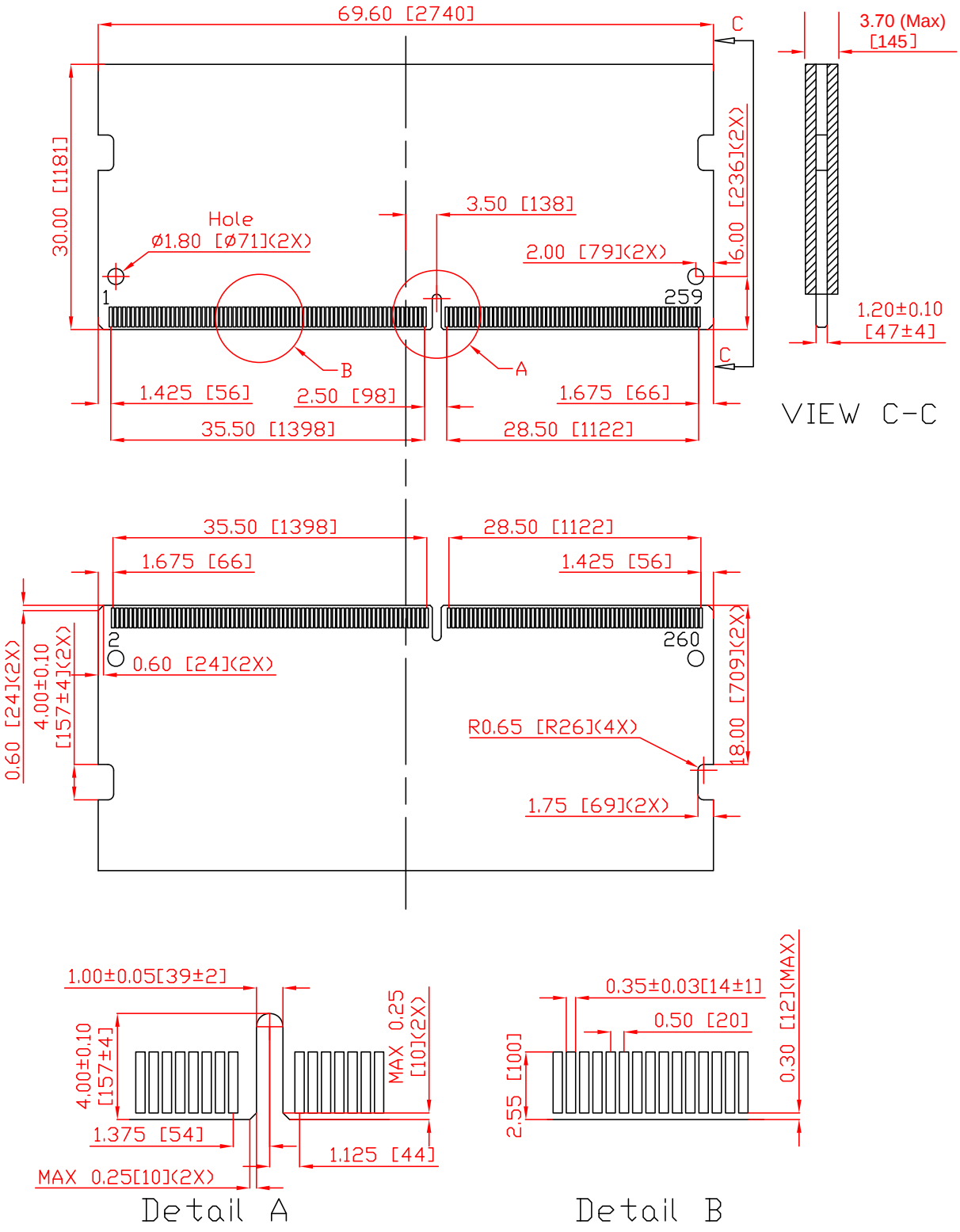
1. DIMM IDD SPEC is based on the condition that de-actived rank(IDLE) is IDD2N. Please refer to Table 1.

[Table1] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
IDD0	IDD0	IDD2N
IDD1	IDD1	IDD2N
IDD2P	IDD2P	IDD2P
IDD2N	IDD2N	IDD2N
IDD2Q	IDD2Q	IDD2Q
IDD3P	IDD3P	IDD3P
IDD3N	IDD3N	IDD3N
IDD4R	IDD4R	IDD2N
IDD4W	IDD4W	IDD2N
IDD5B	IDD5B	IDD2N
IDD6	IDD6	IDD6
IDD7	IDD7	IDD2N
IDD8	IDD8	IDD8

Mechanical Drawing

Unit: mm



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.1	5/5/2014	Initial release	
0.2	11/2/2015	Updated VDDSPD	

Global Presence

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