

***RoHS Compliant***

**2GB DDR2 SDRAM VLP DIMM**

***Product Specifications***

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***Version 1.1***



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## General Description

Apacer **78.A1GAR.40M0C** is a 256M x 64 DDR2 SDRAM (Synchronous DRAM) DIMM. This high-density memory module consists of 16 pieces 128M x 8 bit with 8banks Double Data Rate SDRAMs in FBGA packages mounted on a 240pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each DDR2 SDRAM.

## Ordering Information

| Part Number    | Bandwidth  | Speed Grade | Max Frequency | CAS Latency |
|----------------|------------|-------------|---------------|-------------|
| 78.A1GAR.40M0C | 6.4 GB/sec | 800 Mbps    | 400 MHz       | CL6         |

| Density | Organization | Component  | Rank |
|---------|--------------|------------|------|
| 2GB     | 256M x 64    | 128M x8*16 | 2    |

## Key Parameters

| MT/s        | DDR2-667 | DDR2-800 | DDR2-800 | Unit |
|-------------|----------|----------|----------|------|
| Grade       | -CL5     | -CL5     | -CL6     |      |
| tCK (min)   | 3        | 2.5      | 2.5      | ns   |
| CAS latency | 5        | 5        | 6        | tCK  |
| tRCD (min)  | 15       | 12.5     | 15       | ns   |
| tRP (min)   | 15       | 12.5     | 15       | ns   |
| tRAS (min)  | 45       | 45       | 45       | ns   |
| tRC (min)   | 60       | 57.5     | 60       | ns   |
| CL-tRCD-tRP | 5-5-5    | 5-5-5    | 6-6-6    | tCK  |

## Specifications:

- ◆ JEDEC standard  $1.8V \pm 0.1V$
- ◆ Power Supply  $VDDQ = 1.8V \pm 0.1V$
- ◆ Interface: SSTL\_18
- ◆ Posted CAS
- ◆ Programmable CAS Latency: 4, 5, 6
- ◆ OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- ◆ Fully differential clock operations (CK & /CK)
- ◆ Programmable Burst Length 4 / 8 with both sequential and interleave mode
- ◆ Auto refresh and self refresh supported
- ◆ On Die Termination
- ◆ 8192 refresh cycles / 64ms
- ◆ Serial presence detect with EEPROM
- ◆ Compliance with RoHS
- ◆ Compliance with CE
- ◆ Supports auto-refresh/self-refresh
- ◆ Operating Temperature Range:  
Commercial  $0^{\circ}C \leq TC \leq 85^{\circ}C$
- ◆ Average refresh period  
 $7.8\mu s$  at  $0^{\circ}C \leq TC \leq 85^{\circ}C$   
 $3.9\mu s$  at  $85^{\circ}C \leq TC \leq 95^{\circ}C$

## Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1       | VREF     | 61      | A4       | 121     | VSS      | 181     | VDDQ     |
| 2       | VSS      | 62      | VDDQ     | 122     | DQ4      | 182     | A3       |
| 3       | DQ0      | 63      | A2       | 123     | DQ5      | 183     | A1       |
| 4       | DQ1      | 64      | VDD      | 124     | VSS      | 184     | VDD      |
| 5       | VSS      | 65      | VSS      | 125     | DM0      | 185     | CK0      |
| 6       | /DQS0    | 66      | VSS      | 126     | NC       | 186     | /CK0     |
| 7       | DQS0     | 67      | VDD      | 127     | VSS      | 187     | VDD      |
| 8       | VSS      | 68      | NC       | 128     | DQ6      | 188     | A0       |
| 9       | DQ2      | 69      | VDD      | 129     | DQ7      | 189     | VDD      |
| 10      | DQ3      | 70      | A10(AP)  | 130     | VSS      | 190     | BA1      |
| 11      | VSS      | 71      | BA0      | 131     | DQ12     | 191     | VDDQ     |
| 12      | DQ8      | 72      | VDDQ     | 132     | DQ13     | 192     | /RAS     |
| 13      | DQ9      | 73      | /WE      | 133     | VSS      | 193     | /S0      |
| 14      | VSS      | 74      | /CAS     | 134     | DM1      | 194     | VDDQ     |
| 15      | /DQS1    | 75      | VDDQ     | 135     | NC       | 195     | ODT0     |
| 16      | DQS1     | 76      | /S1      | 136     | VSS      | 196     | A13      |
| 17      | VSS      | 77      | ODT1     | 137     | CK1      | 197     | VDD      |
| 18      | NC       | 78      | VDDQ     | 138     | /CK1     | 198     | VSS      |
| 19      | NC       | 79      | VSS      | 139     | VSS      | 199     | DQ36     |
| 20      | VSS      | 80      | DQ32     | 140     | DQ14     | 200     | DQ37     |
| 21      | DQ10     | 81      | DQ33     | 141     | DQ15     | 201     | VSS      |
| 22      | DQ11     | 82      | VSS      | 142     | VSS      | 202     | DM4      |
| 23      | VSS      | 83      | /DQS4    | 143     | DQ20     | 203     | NC       |
| 24      | DQ16     | 84      | DQS4     | 144     | DQ21     | 204     | VSS      |
| 25      | DQ17     | 85      | VSS      | 145     | VSS      | 205     | DQ38     |
| 26      | VSS      | 86      | DQ34     | 146     | DM2      | 206     | DQ39     |
| 27      | /DQS2    | 87      | DQ35     | 147     | NC       | 207     | VSS      |
| 28      | DQS2     | 88      | VSS      | 148     | VSS      | 208     | DQ44     |
| 29      | VSS      | 89      | DQ40     | 149     | DQ22     | 209     | DQ45     |
| 30      | DQ18     | 90      | DQ41     | 150     | DQ23     | 210     | VSS      |

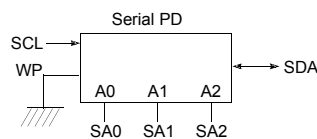
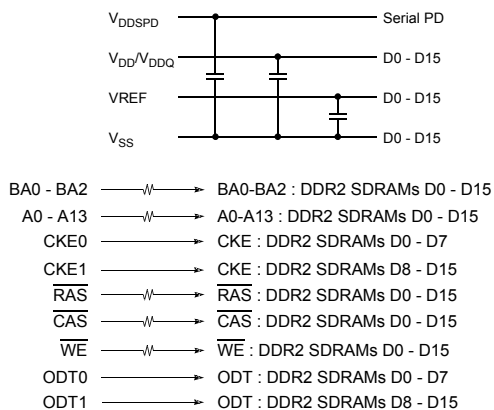
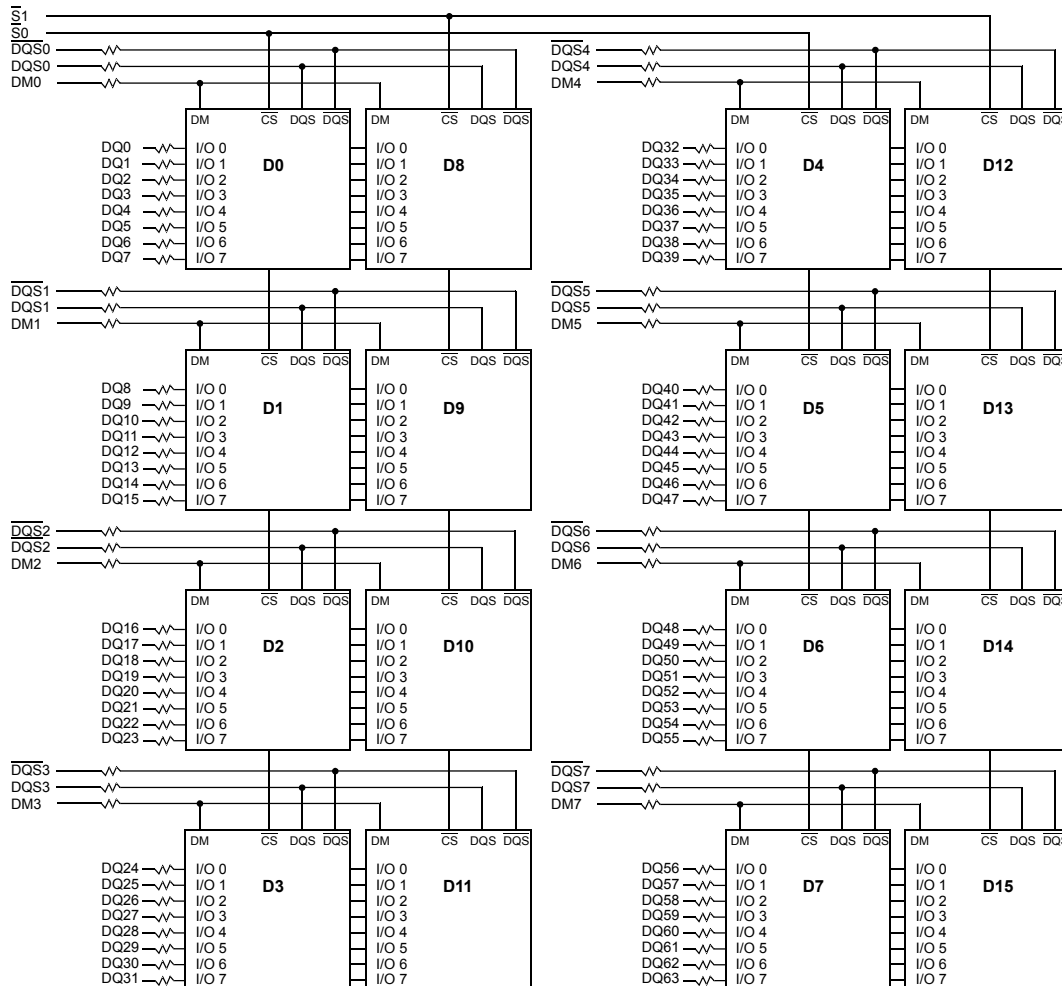
| Pin No. | Pin name  | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|-----------|---------|----------|---------|----------|---------|----------|
| 31      | DQ19      | 91      | VSS      | 151     | VSS      | 211     | DM5      |
| 32      | VSS       | 92      | /DQS5    | 152     | DQ28     | 212     | NC       |
| 33      | DQ24      | 93      | DQS5     | 153     | DQ29     | 213     | VSS      |
| 34      | DQ25      | 94      | VSS      | 154     | VSS      | 214     | DQ46     |
| 35      | VSS       | 95      | DQ42     | 155     | DM3      | 215     | DQ47     |
| 36      | /DQS3     | 96      | DQ43     | 156     | NC       | 216     | VSS      |
| 37      | DQS3      | 97      | VSS      | 157     | VSS      | 217     | DQ52     |
| 38      | VSS       | 98      | DQ48     | 158     | DQ30     | 218     | DQ53     |
| 39      | DQ26      | 99      | DQ49     | 159     | DQ31     | 219     | VSS      |
| 40      | DQ27      | 100     | VSS      | 160     | VSS      | 220     | CK2      |
| 41      | VSS       | 101     | SA2      | 161     | NC(CB4)* | 221     | /CK2     |
| 42      | NC(CB0)*  | 102     | NC(TEST) | 162     | NC(CB5)* | 222     | VSS      |
| 43      | NC(CB1)*  | 103     | VSS      | 163     | VSS      | 223     | DM6      |
| 44      | VSS       | 104     | /DQS6    | 164     | NC(DM8)* | 224     | NC       |
| 45      | NC(DQS8)* | 105     | DQS6     | 165     | NC       | 225     | VSS      |
| 46      | NC(DQS8)* | 106     | VSS      | 166     | VSS      | 226     | DQ54     |
| 47      | VSS       | 107     | DQ50     | 167     | NC(CB6)* | 227     | DQ55     |
| 48      | NC(CB2)*  | 108     | DQ51     | 168     | NC(CB7)* | 228     | VSS      |
| 49      | NC(CB3)*  | 109     | VSS      | 169     | VSS      | 229     | DQ60     |
| 50      | VSS       | 110     | DQ56     | 170     | VDDQ     | 230     | DQ61     |
| 51      | VDDQ      | 111     | DQ57     | 171     | CKE1     | 231     | VSS      |
| 52      | CKE0      | 112     | VSS      | 172     | VDD      | 232     | DM7      |
| 53      | VDD       | 113     | /DQS7    | 173     | NC(A15)* | 233     | NC       |
| 54      | NC(BA2)*  | 114     | DQS7     | 174     | NC(A14)* | 234     | VSS      |
| 55      | NC        | 115     | VSS      | 175     | VDDQ     | 235     | DQ62     |
| 56      | VDDQ      | 116     | DQ58     | 176     | A12      | 236     | DQ63     |
| 57      | A11       | 117     | DQ59     | 177     | A9       | 237     | VSS      |
| 58      | A7        | 118     | VSS      | 178     | VDD      | 238     | VDDSPD   |
| 59      | VDD       | 119     | SDA      | 179     | A8       | 239     | SA0      |
| 60      | A5        | 120     | SCL      | 180     | A6       | 240     | SA1      |

1. Pin173 Pin174 are reserved for 2Gb / 4Gb comp. base Unbuffered DIMM.
2. The \* pin is not connected on this un-buffer memory module products

## Pin Descriptions

| Pin Name | Description                                               |
|----------|-----------------------------------------------------------|
| Ax       | SDRAM address bus                                         |
| BAx      | SDRAM bank select                                         |
| /RAS     | SDRAM row address strobe                                  |
| /CAS     | SDRAM column address strobe                               |
| /WE      | SDRAM write enable                                        |
| /Sx      | DIMM Rank Select Lines                                    |
| CKEx     | SDRAM clock enable lines                                  |
| ODTx     | On-die termination control lines                          |
| DQx      | DIMM memory data bus                                      |
| CBx      | DIMM ECC check bits                                       |
| DQSx     | SDRAM data strobes(positive line of differential pair)    |
| /DQSx    | SDRAM data strobes(negative line of differential pair)    |
| DMx      | SDRAM data masks high data strobes(x8-based X72 DIMMs)    |
| CKx      | SDRAM clocks(positive line of differential pair)          |
| /CKx     | SDRAM clocks(negative line of differential pair)          |
| SCL      | I2C serial bus clock for EEPROM                           |
| SDA      | I2C serial bus data line for EEPROM                       |
| SAx      | I2C slave address select for EEPROM                       |
| VDD      | SDRAM core power supply                                   |
| VDDQ     | SDRAM I/O Driver power supply                             |
| VREF     | SDRAM I/O reference supply                                |
| VSS      | Power supply return(ground)                               |
| VDDSPD   | Serial EEPROM positive power supply                       |
| NC       | Spare pins(no connect)                                    |
| TEST     | Used by memory bus analysis tools(unused on memory DIMMS) |
| RESET    | Set DRAMs to Known State                                  |

# Functional Block Diagram



| * Clock Wiring |               |
|----------------|---------------|
| Clock Input    | DDR2 SDRAMs   |
| *CK0/CK0       | 4 DDR2 SDRAMs |
| *CK1/CK1       | 6 DDR2 SDRAMs |
| *CK2/CK2       | 6 DDR2 SDRAMs |

\*Wire per Clock Loading  
Table/Wiring Diagrams

- Notes :**
1. DQ, DM, DQS/DQS resistors : 22 Ohms " 5%.
  2. BAx, Ax, RAS, CAS, WE resistors : 3 Ohms " 5%.



## Absolute Maximum Ratings

| Parameter                           | Symbol                             | Description     | Units |
|-------------------------------------|------------------------------------|-----------------|-------|
| Voltage on VDD pin relative to Vss  | V <sub>DD</sub>                    | - 1.0 V ~ 2.3 V | V     |
| Voltage on VDDQ pin relative to Vss | V <sub>DDQ</sub>                   | - 0.5 V ~ 2.3 V | V     |
| Voltage on any pin relative to Vss  | V <sub>IN</sub> , V <sub>OUT</sub> | - 0.5 V ~ 2.3 V | V     |
| Storage Temperature                 | TSTG                               | -55 to +100     | °C    |

Notes:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. .

## DRAM Component Operating Temperature Range

| Symbol            | Parameter                          | Rating   | Units | Notes |
|-------------------|------------------------------------|----------|-------|-------|
| T <sub>OPER</sub> | Normal Operating Temperature Range | 0 to 85  | °C    | 1,2   |
|                   | Extended Temperature Range         | 85 to 95 | °C    | 1,3   |

### Notes:

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported during operation, the DRAM case temperature must be maintained between 0°C - 85°C under all operating Conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs.
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

# Operating Conditions

## Recommended DC Operating Conditions – DDR2 (1.8V) operation

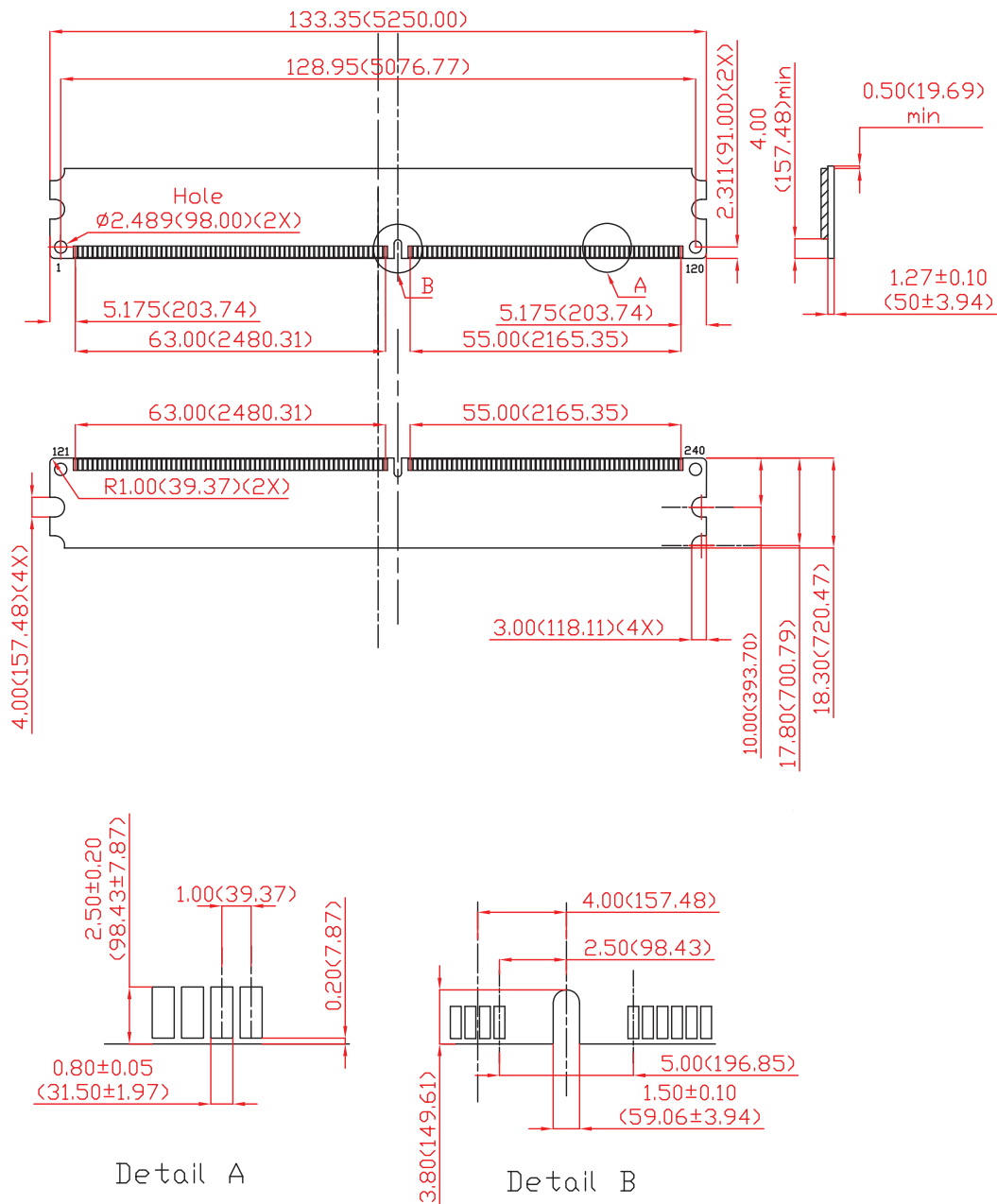
| Symbol | Parameter                 | Rating |      |      | Units |
|--------|---------------------------|--------|------|------|-------|
|        |                           | Min.   | Typ. | Max. |       |
| VDD    | Supply Voltage            | 1.7    | 1.8  | 1.9  | V     |
| VDDQ   | Supply Voltage for Output | 1.7    | 1.8  | 1.9  | V     |

### Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

# Mechanical Drawing

Unit: mm / (Mils)



Tolerances:  $\pm 0.15$ mm unless otherwise specified

## Revision History

| Revision | Date       | Description                  | Remark |
|----------|------------|------------------------------|--------|
| 0.9      | 08/28/2012 | Official release             |        |
| 1.0      | 08/29/2012 | release                      |        |
| 1.1      | 07/23/2013 | Changed headquarters address |        |

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