RoHS Recast Compliant

Industrial MicroSD

R1 Product Specifications

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Version 1.2

Apacer Technology Inc.
1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

FEATURES:

- **Fully Compatible with SD Card Specifications 3.0, 2.0 and 1.1**
  - Part 1, Physical Layer Specification, Ver 3.01 Final
  - Part 2, File System Specification, Ver 3.00
  - Part 3, Security Specification, Ver 3.00 Final
- **Capacity**
  - SD 2.0: 1, 2 GB
  - SD 3.0: 4, 8 GB
- **Performance***
  - Sustained Read: Up to 34 MB/sec
  - Sustained Write: Up to 28 MB/sec
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Standard Interface**
  - 8-pins SD interface
- **NAND Flash Type: SLC**
- **Flash Management**
  - Flash bad-block management
  - Built-in advanced ECC algorithms
  - Power management
  - S.M.A.R.T.
  - Wear-leveling algorithms
- **Temperature Range**
  - Operating temperature: -40°C to 85°C
  - Storage temperature: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption***
  - Operating: 115 mA
  - Standby: 265 µA
- **Dimensions:** 15㎜(L) x 11㎜(W) x 1㎜(H)
- **RoHS Recast Compliant (2011/65/EU)**

*Performance values presented here are typical and may vary depending on settings and platforms.

TABLE OF CONTENTS

1. General Description 3

1.1 Product Function Block 3
1.2 Functional Description 4
1.2.1 Flash Management *4*
1.2.2 ECC Algorithms *4*
1.2.3 Power Management *4*
1.2.4 S.M.A.R.T. *4*
1.2.5 Wear Leveling *5*

2. Electrical Characteristics 6

2.1 Card Architecture 6
2.2 Pin Assignment 6
2.3 Capacity Specifications 7
2.4 Performance Specifications 7
2.5 Electrical Specifications 7

3. Physical Characteristics 8

3.1 Physical Dimensions 8
3.2 Environmental Specifications 10
3.2.1 Climatic Testing *10*
3.2.2 Durability Testing *11*

4. AC Characteristics 12

4.1 MicroSD Interface Timing (Default) 12
4.2 MicroSD Interface Timing (High Speed Mode) 13
4.3 MicroSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input 15
4.3.1 Clock Timing *15*
4.3.2 Card Input Timing *15*
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50) *16*
4.3.4 Output Timing of Variable Window (SDR104) *16*
4.3.5 SD Interface Timing (DDR50 Mode) *17*
4.3.6 Bus Timings – Parameters Values (DDR50 Mode) *18*

5. S.M.A.R.T. 19

5.1 SMART Getting Flow Chart 19
5.2 The Entry Pattern and Leave Pattern 20
5.2.1 Entry Pattern (LBA: 0) *20*
5.2.2 Leave Pattern (LBA: 0) *20*
5.3 SMART Returned Table 21

6. Product Ordering Information 22

6.1 Product Code Designations 22
6.2 Valid Combinations 23

1. General Description

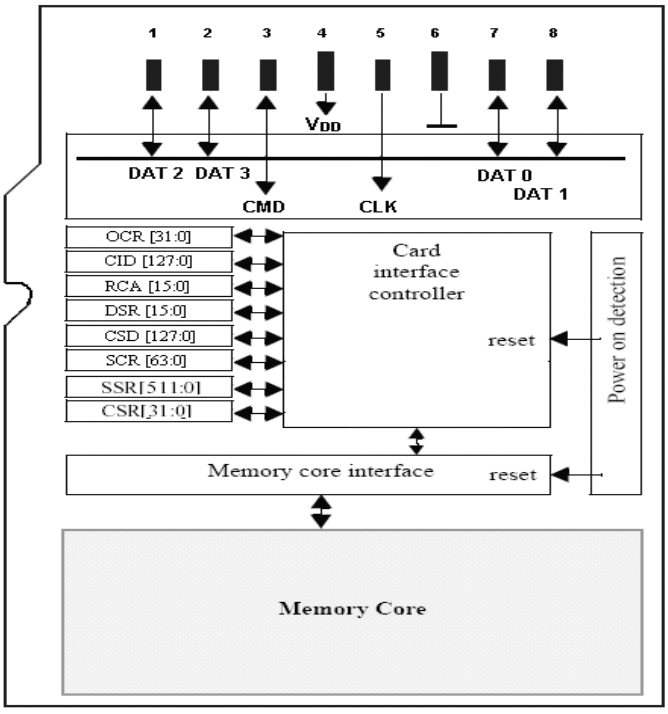
As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's MicroSD card is designed specifically for multiple applications by offering high endurance, reliability, and agility, where extreme flexibility, endurance, data integrity, and exceptionally transmission are required.

The MicroSD card fully complies with SD Card Association standard. The Command List is compatible with [Part 1 Physical Layer Specification Ver3.1 Final] definitions, while the Card Capacity of Non-secure Area, Secure Area supports [Part 3 Security Specification Ver3.0 Final] Specifications. The card allows selection of either SD or SPI mode for compatibility in data communication.

The card also comes with endurance features for data error detection and correction.

1.1 Product Function Block

The MicroSD contains a card controller and a memory core for the SD standard interface.



1.2 Functional Description

The MicroSD device contains a high level, intelligent flash management that provides many capabilities including:

- Flash bad-block management
- ECC algorithms
- Power management
- S.M.A.R.T.
- Wear leveling algorithms

1.2.1 Flash Management

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block including user data space and spare block.

The MicroSD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD will replace this bad bit with a spare bit within the sector header. If necessary, the MicroSD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.2.2 ECC Algorithms

The powerful ECC algorithms will enhance flash block use rate and whole device life. The SD controller supports up to 68bits ECC circuits to protect data transfer.

1.2.3 Power Management

A power saving feature of the MicroSD is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the MicroSD will cause it to exit sleep mode and response to the master.

1.2.4 S.M.A.R.T.

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

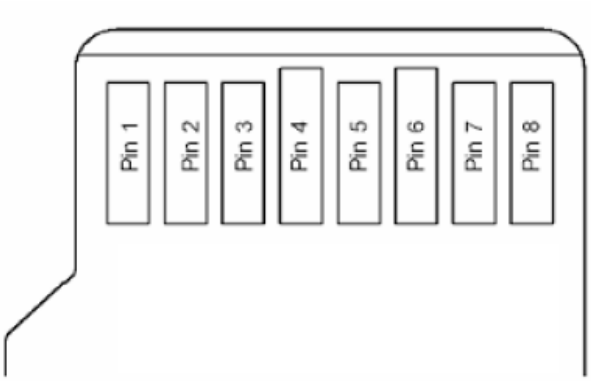
1.2.5 Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Apacer provides wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

2. Electrical Characteristics

2.1 Card Architecture



2.2 Pin Assignment

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data Line[Bit 2]	RSV	Reserved
2	CD/DAT3 [2]	Card Detect/Data Line[Bit 3]	CS	Chip Select (neg true)
3	CMD	Command/Response	DI	Data In
4	VDD	Supply Voltage	VDD	Supply Voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply Voltage Ground	VSS	Supply Voltage Ground
7	DAT0	Data Line[Bit 0]	DO	Data Out
8	DAT1	Data Line[Bit 1]	RSV	Reserved

2.3 Capacity Specifications

The following table shows the specific capacity for the SD card.

Capacity	Total Bytes
1 GB	969,605,120
2 GB	1,938,489,344
4 GB	3,875,504,128
8 GB	7,751,041,024

Note: total bytes are viewed under Windows operating system and were measured by SD format too.

2.4 Performance Specifications

Performances of the SD card are shown in the table below.

Modes \ Capacity	1 GB	2 GB	4 GB	8 GB
Read (MB/s)	23	23	34	33
Write (MB/s)	16	18	28	28

Note: results may vary depending on settings and platforms.

2.5 Electrical Specifications

Operating Voltage

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.6	V

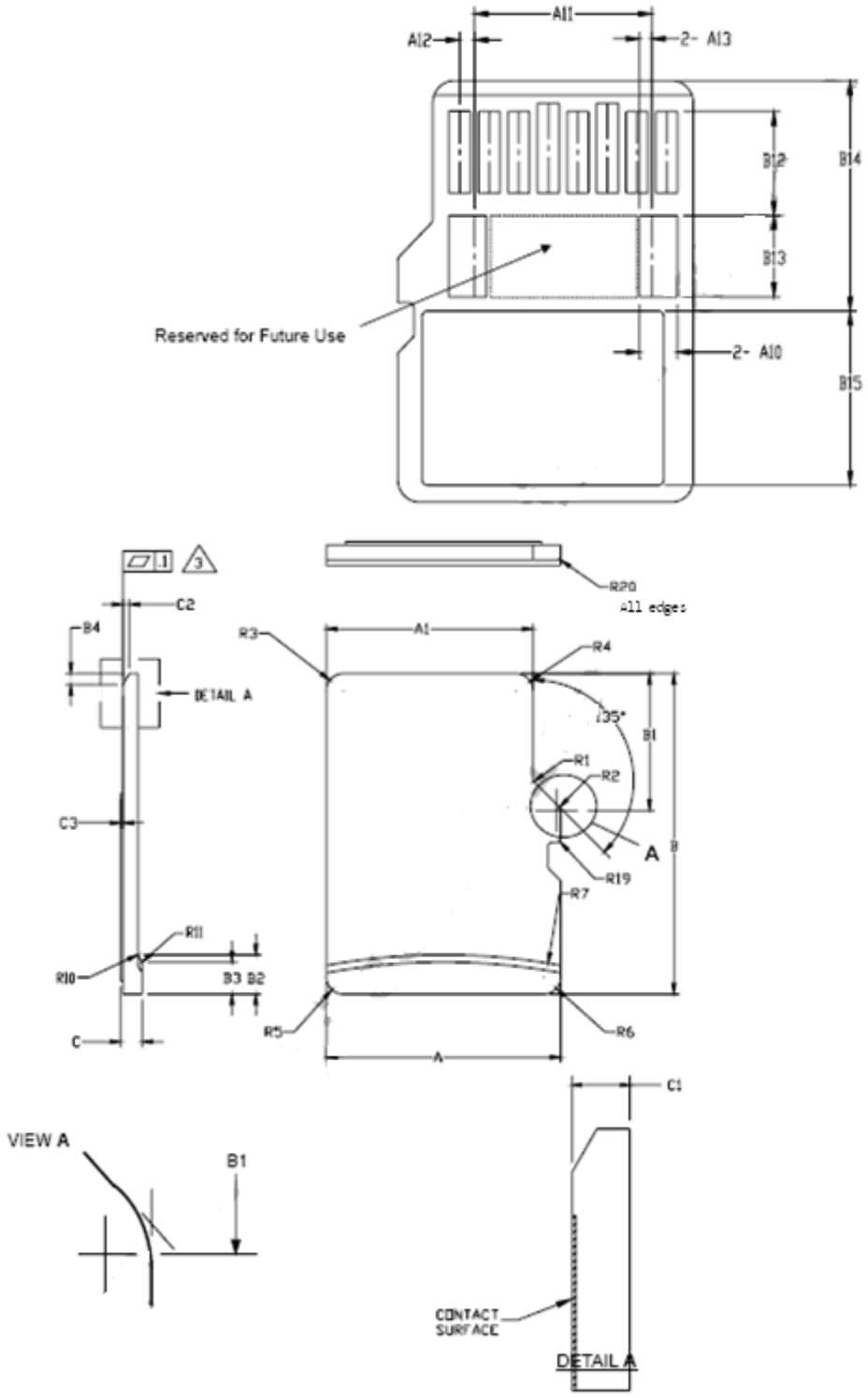
Power Consumption

Modes \ Capacity	1 GB	2 GB	4 GB	8 GB
Operating (mA)	110	110	110	115
Standby (µA)	160	160	260	265

Note: results may vary depending on settings and platforms.

3. Physical Characteristics

3.1 Physical Dimensions



	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS ARE IN MILLIMETERS.

3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

3.2 Environmental Specifications

3.2.1 Climatic Testing

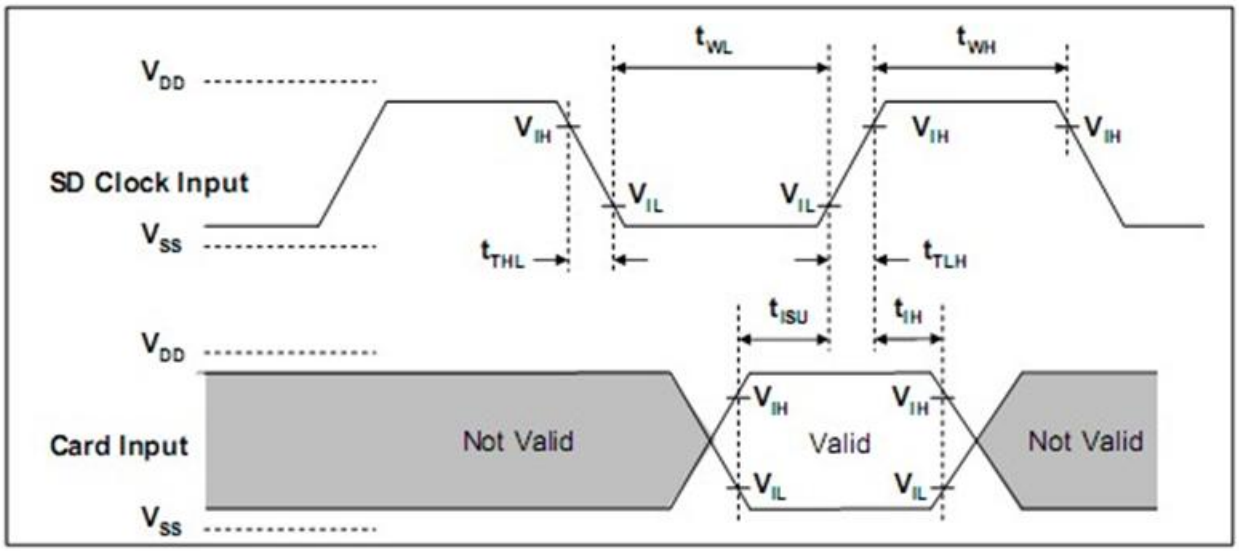
Test Item	DUT State	Test Condition	
		Temperature	Duration
High Temperature	Storage	85℃	500 Hours
Low Temperature	Storage	-40℃	500 Hours
Temperature Cycling	Storage	-40℃ ~ 85℃ 30min hold each	50 Cycles

3.2.2 Durability Testing

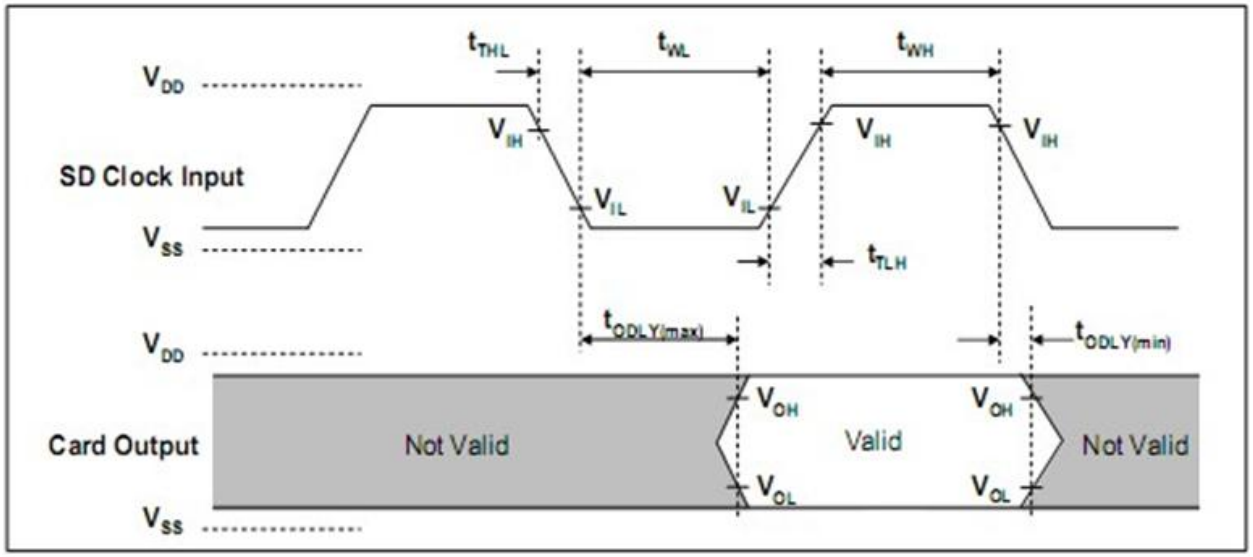
Test Item	Descriptions
Insertion/Removal	10,000 cycles
Bending	10nt/5 times for 6 faces and 4 corners (each drop was performed 3 times, total of 30 drops)
Electrostatic Discharge	Contact discharge: HCP & VCP Air discharge: ALL – VSS (±), ALL – VCC (±), VCC – VSS (±), ALL – ALL (±)
Ultraviolet Radiation	Units are non-operating. UVB bandwidth：313 nm. Test irradiation：0.63 w/m²/nm. Radiation cycle：Radiation on for 4 hours at temperature 60°C, then radiation off for 4 hours at temperature 60°C. Number of cycle：6 cycles. Duration of test：48 hours
Drop	1.5 m free fall, 10 times
Salt Water Spray	3+/-1%NaCl; 35℃; 24hrs
Torque	0.1 N-m or ± 2.5 degree 5 time; 30 sec/direction

4. AC Characteristics

4.1 MicroSD Interface Timing (Default)



Card input Timing (Default Speed Card)

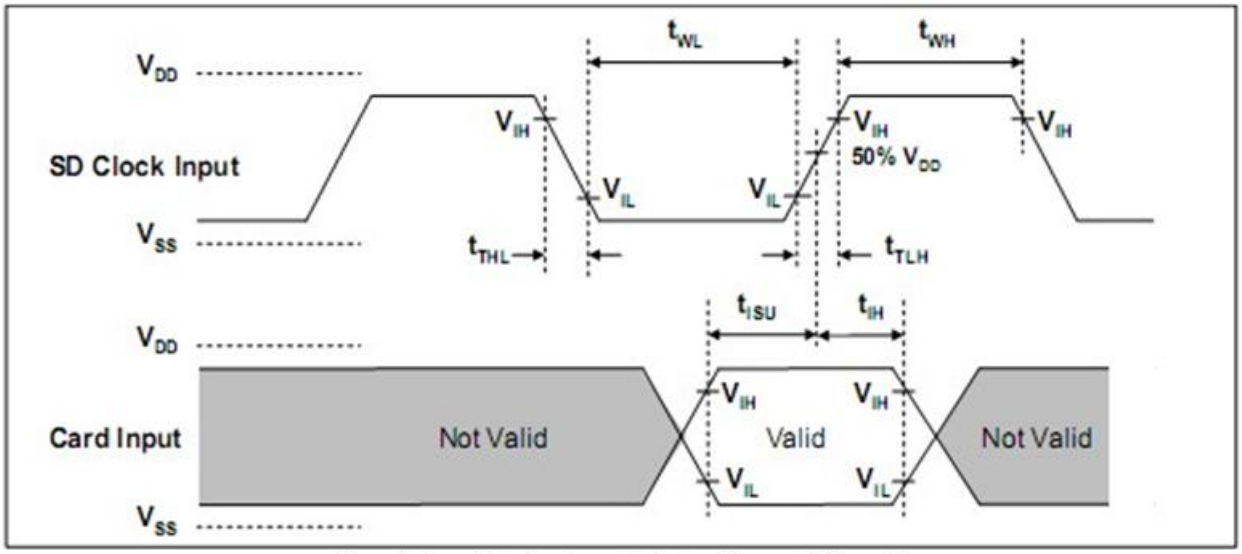


Card Output Timing (Default Speed Mode)

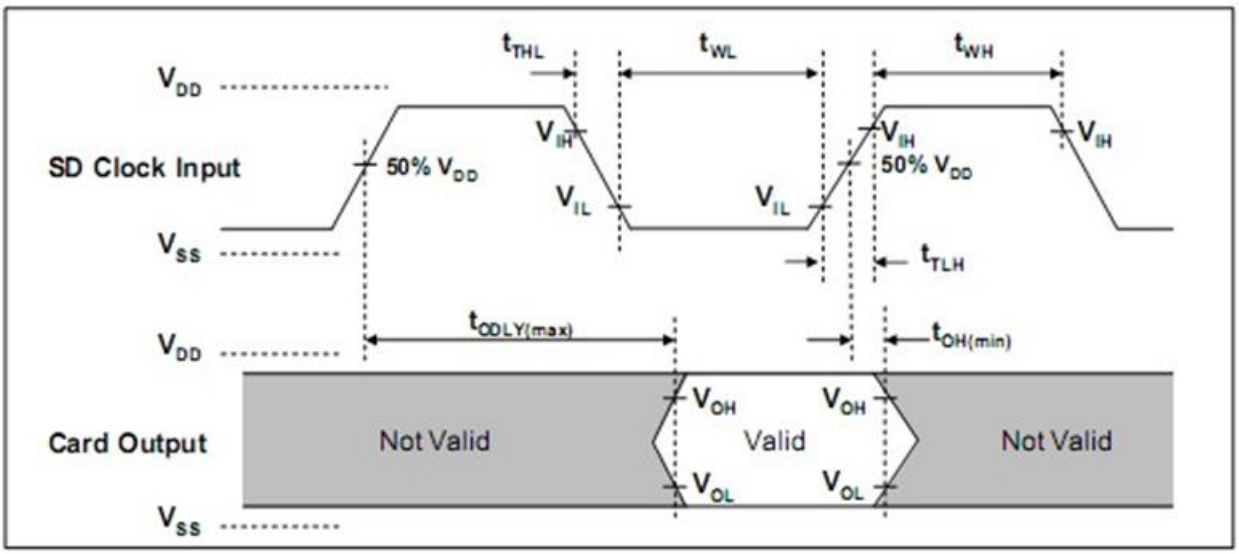
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	25	MHz	C_{card} ≤ 10 pF (1 card)
f_{OD}	Clock frequency identification	0[(1)]/100	400	KHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	10	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	5	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TH}	Input hold time	5	-	ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer mode	0	14	ns	C_L ≤ 40 pF (1 card)
t_{OH}	Output hold time	0	50	ns	C_L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 MicroSD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



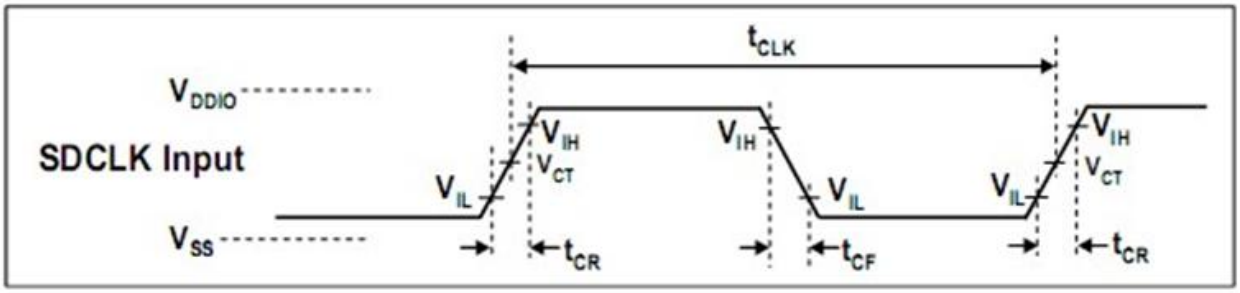
Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	Ccard ≤ 10 pF (1 card)
t_{WL}	Clock low time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{WH}	Clock high time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	Ccard ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	3	ns	Ccard ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	Ccard ≤ 10 pF (1 card)
t_{TH}	Input hold time	2	-	ns	Ccard ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 MicroSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

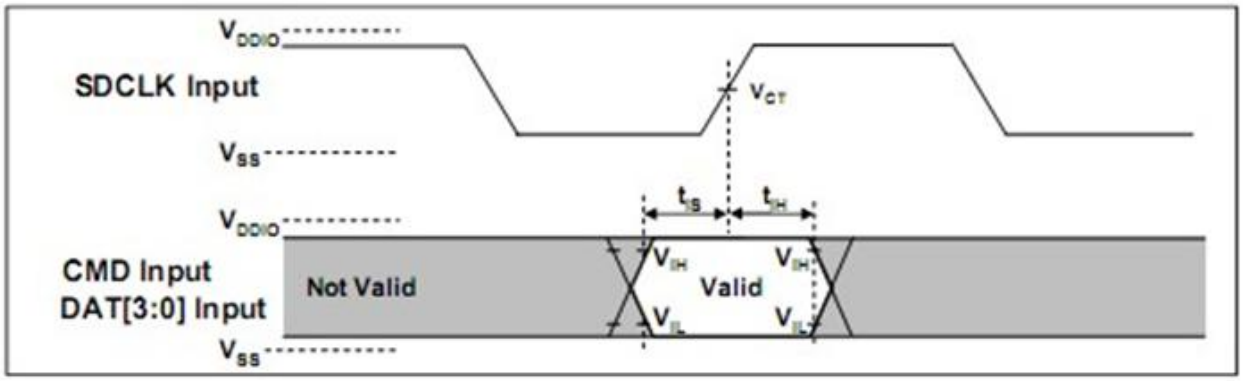
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

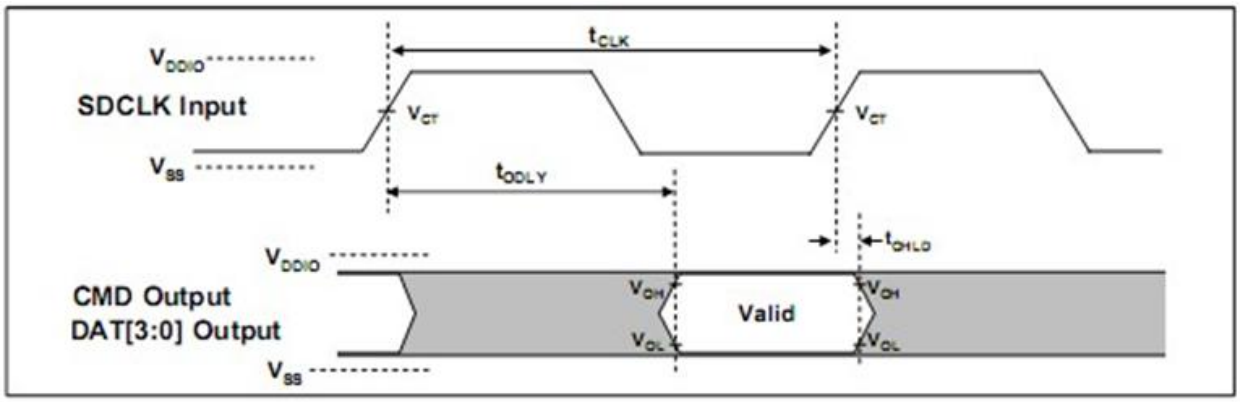
4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
SYMBOL	**MIN**	**MAX**	**UNIT**	**SDR12, SDR25 and SDR50 MODES**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

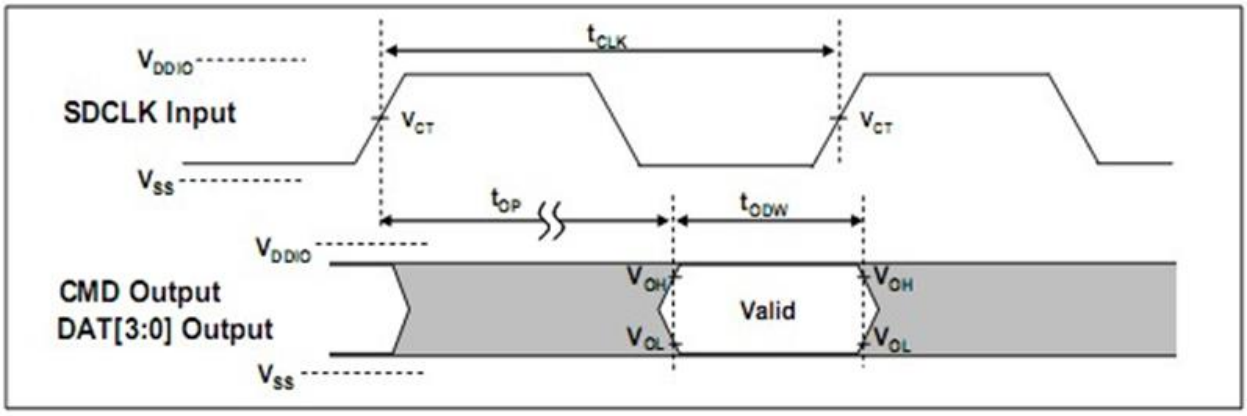
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). CL=15pF

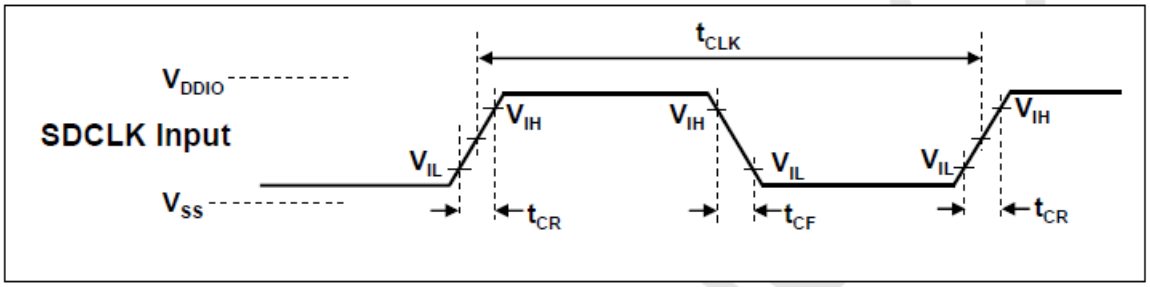
4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window

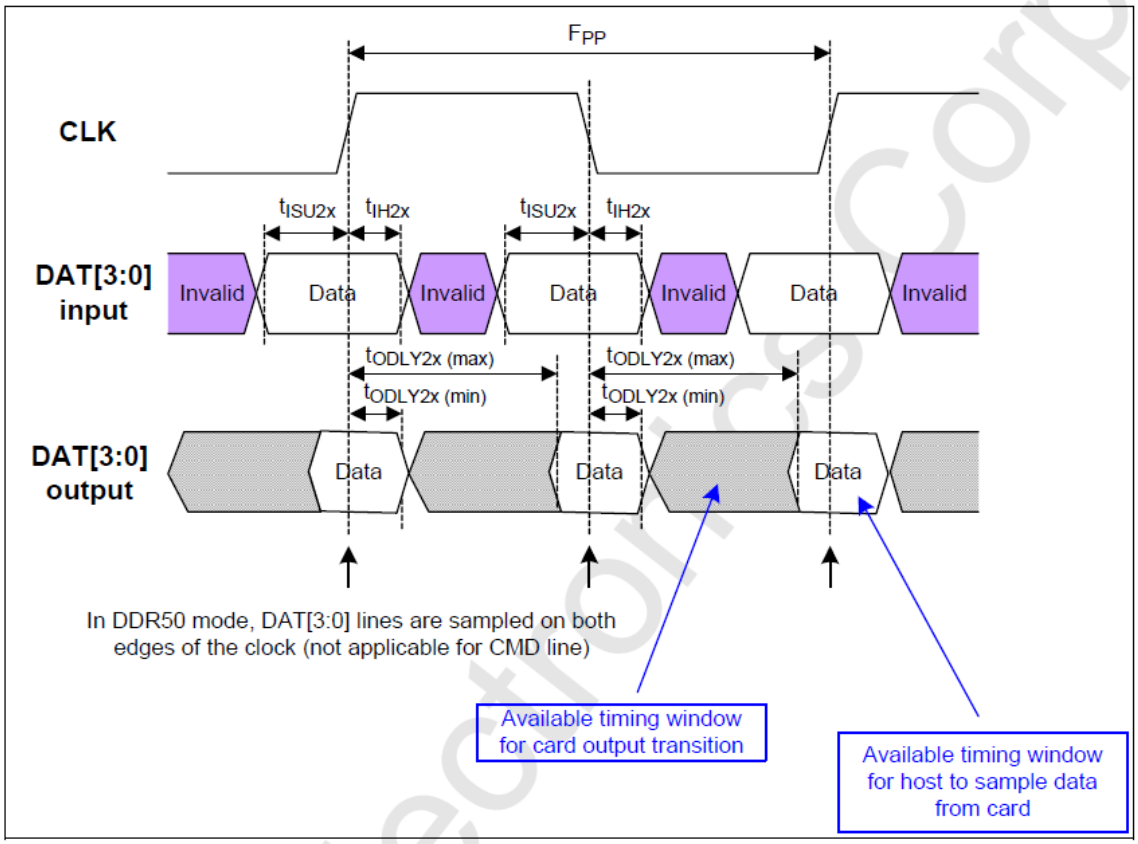
SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	C_L≤30 pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	C_L≤25 pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)

5. S.M.A.R.T.

5.1 SMART Getting Flow Chart

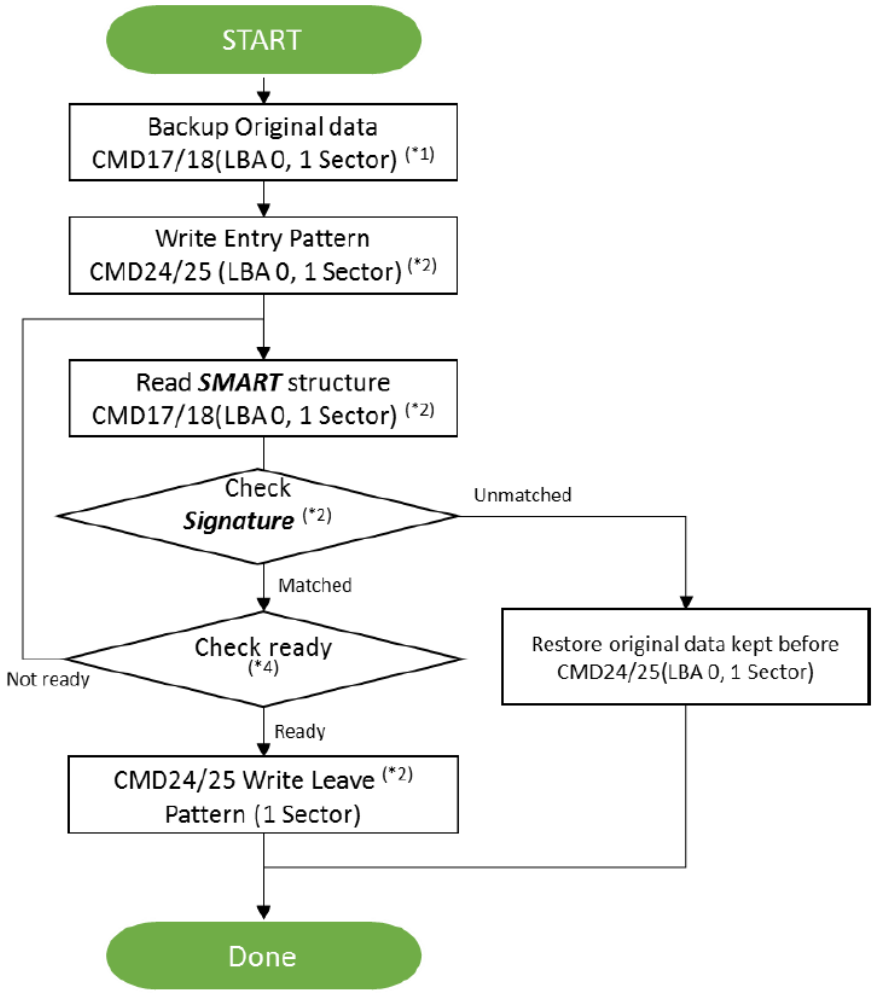


Figure 5-1 SMART Getting Flow Chart

(*1) Due to the SMART Read Flow is started by a **Write** command, the **backup-and-restore** activity is suggested to save the data in other storage media that aren't R1 products.

(*2) The **Arguments** of the SD CMD24/CMD25/CMD17/CMD18 (or the **LBA** of the SCSI Read/Write) should be **0**.

(*3) The first 3 bytes of the Read command returned data, called **Signature**, should be **53h**, **49h**and **30h**. It confirms that the hardware accepted the SMART Entry Pattern for starting the SMART process.

(*4) After issuing Entry Pattern, the device starts to process preparing the SMART data. It may takes some time so that the AP should issue the Read Command repeatedly and check byte[73] of the returned data. **When byte[73] returned 1 it indicates that the data is busy and 0 for the data is ready**. Until byte[73] returned as ready, the others bytes in the retuned data is available simultaneously.

5.2 The Entry Pattern and Leave Pattern

5.2.1 Entry Pattern (LBA: 0)

N	N+0	N+1	N+2	N+3	N+4	N+5	N+6	N+7
000	36h	39h	36h	36h	38h	33h	30h	33h
007 : : 246	All Zero (240 Bytes)							
247	33h	30h	33h	38h	36h	36h	39h	36h
256	02h	39h	36h	36h	38h	33h	30h	33h
264 : : 503	All Zero (240 Bytes)							
504	33h	30h	33h	38h	36h	36h	39h	36h

5.2.2 Leave Pattern (LBA: 0)

N	N+0	N+1	N+2	N+3	N+4	N+5	N+6	N+7
000	33h	30h	33h	38h	36h	36h	39h	36h
007 : : 246	All Zero (240 Bytes)							
247	36h	39h	36h	36h	38h	33h	30h	33h
256	33h	30h	33h	38h	36h	36h	39h	36h
264 : : 503	All Zero (240 Bytes)							
504	02h	39h	36h	36h	38h	33h	30h	33h

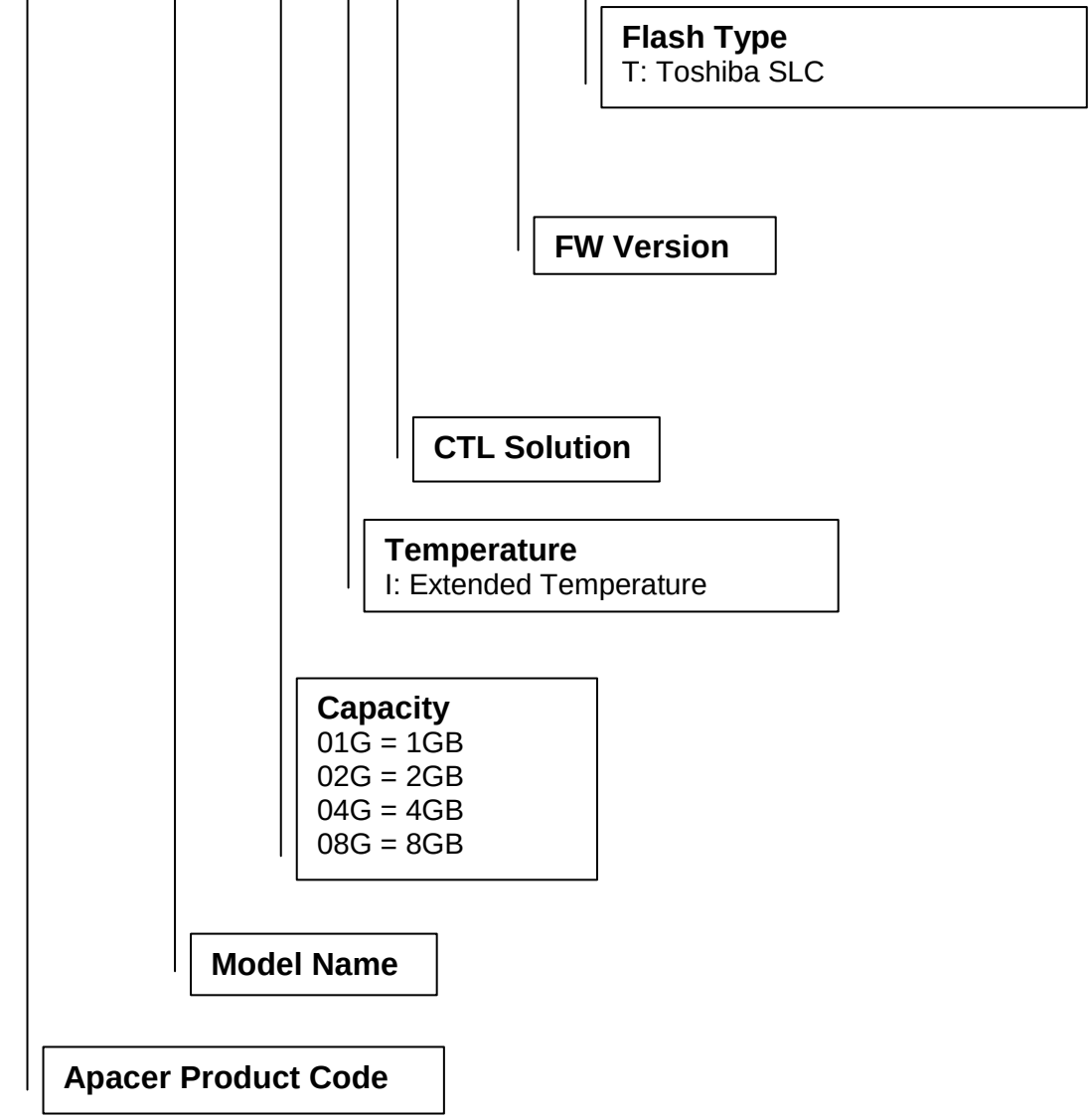
5.3 SMART Returned Table

Location	Digits	Name	Description
0-2	3	Signature	53h 49h 30h
3-18	16	Reserved	Reserved
19-34	16	Reserved	Reserved
35	1	Flash Type	0: SLC, 1: MLC
36-41	6	Flash ID	Flash ID Numbers
42-45	4	Flash PE Cycle	Flash P/E Cycle Times
46-49	4	Reserved	Reserved
50-51	2	Initial Bad Block Count	Physical number of bad blocks marked by factory
52-53	2	Later Bad VB	The number of bad blocks in virtual unit marked at run time
54-55	2	Spare Block Count	Spare Block Count
56	1	Reserved	Reserved
57-60	4	Total Erase Count	0 - 4294967295
61-64	4	Abnormal Shut Down Count	The number of abnormal unplug/power down times detected by the device
65-68	4	Power Cycle Count	The number of re-plug times
69-70	2	Reserved	Reserved
71	1	Total CE Count	NAND CE number of the device
72	1	VB Multiplier	The multiplier to convert Virtual Block Numbers to Physical Block Numbers
73	1	SMART Data Ready	Returns 1 for indicating preparing data; 0 for indicating that the data is ready
74-75	2	MP Version (High)	3rd number of the MP Version in 16 bits
76-77	2	MP Version (Low)	4th number of the MP Version in 16 bits
78-81	4	Total Virtual Blocks	The Total Physical Blocks / VB Multiplier
82-511	430	Reserved	Reserved

6. Product Ordering Information

6.1 Product Code Designations

AP – MSD xxG I E – AA T



6.2 Valid Combinations

Capacity	AP/N
1GB	AP-MSD01GIE-AAT
2GB	AP-MSD02GIE-AAT
4GB	AP-MSD04GIE-AAT
8GB	AP-MSD08GIE-AAT

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	12/22/2015
1.1	- Added S.M.A.R.T. chapter - Revised product ordering information	1/13/2016
1.2	Specified supported capacity for SD 2.0 and SD 3.0 respectively	1/18/2016

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: 886-2-2267-8000
Fax: 886-2-2267-2261
amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9568
sa@apacerus.com

Japan

Apacer Technology Corp.
5F, Matsura Bldg., Shiba, Minato-Ku
Tokyo, 105-0014, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe

Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-267-0000#6199
sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD, Shanghai, 200051, China
Tel: 86-21-6228-9939
Fax: 86-21-6228-9936
sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd,
Unit No.201, “Brigade Corner”, 7th Block Jayanagar,
Yediyur Circle, Bangalore – 560082, India
Tel: 91-80-4152-9061
Fax: 91-80-4170-0215
sales_india@apacer.com