Halogen Free & RoHS Recast Complaint

CompactFlash Series 6

CF6H Product Specifications

March 16th, 2015

Version 1.1

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Features:

- **CompactFlash Association Specification Revision 6.x Standard Interface**
  - ATA command set compatible
  - Backward compatible with CompactFlash Specification Version 3.x, 4.x and 6.x
  - Compatible with PC Card Standard Release 8.0
  - IDE standard interface
  - ATA transfer mode supports:
    PIO Mode 6
    Multiword DMA Mode 4
    Ultra DMA Mode 7
    PCMCIA UDMA Mode 5
- **Capacities**
  - 512 MB,
  - 1, 2, 4, 8, 16, 32, 64 GB
- **Performance***
  - Sustained read: Up to 80 MB/sec
  - Sustained write: Up to 75 MB/sec
- **Flash Management**
  - Wear-leveling
  - Built-in BCH ECC ,
- **NAND Flash Type: SLC**
- **Temperature ranges**
  - Operating:
    Standard: 0°C to 70°C
    Extended: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Operating voltage for read and write**
  - 3.3V / 5V
- **Power consumption (typical)***
  - Active mode: 250mA/5.0V
  - Standby mode: 1.5 mA/5.0V
- **Connector Type**
  - 50 pins female
- **Physical Dimensions**
  - 36.4mm x 42.8mm x 3.3mm
- **RoHS**

*Performance and power consumption may vary depending on capacities, flash configuration or host system settings.

Table of Contents

1. General Description

Apacer's value-added Industrial CompactFlash Card offers high performance, high reliability and power-efficient storage. Regarding standard compliance, this CompactFlash Card complies with CompactFlash specification revision 6.0, supporting transfer modes up to Programmed Input Output (PIO) Mode 6, Multi-word Direct Memory Access (DMA) Mode 4, Ultra DMA Mode 7, and PCMCIA Ultra DMA Mode 5.

For power efficiency, this industrial CompactFlash card supports Power Management which allows the device to switch among Standby, Active, Idle and Sleep modes.

Apacer 's CompactFlash technology is designed for applications in Point of Sale (POS) terminals, telecom, IP-STB, mobile instruments, surveillance systems, industrial PCs and other embedded applications.

1.2 Flash Management

1.2.1 Wear-leveling algorithms

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

1.2.2 Flash Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

1.2.3 Error Correction/Detection

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, Compact Flash Card applies the BCH ECC Algorithm, which can detect and correct errors up to 68-bit in 1K byte data during Read process, ensure data been read correctly, as well as protect data from corruption.

2. Functional Block

The CompactFlash Card (CFC) includes a controller and flash media, as well as the CompactFlash standard interface. Figure 2-1 shows the functional block diagram.

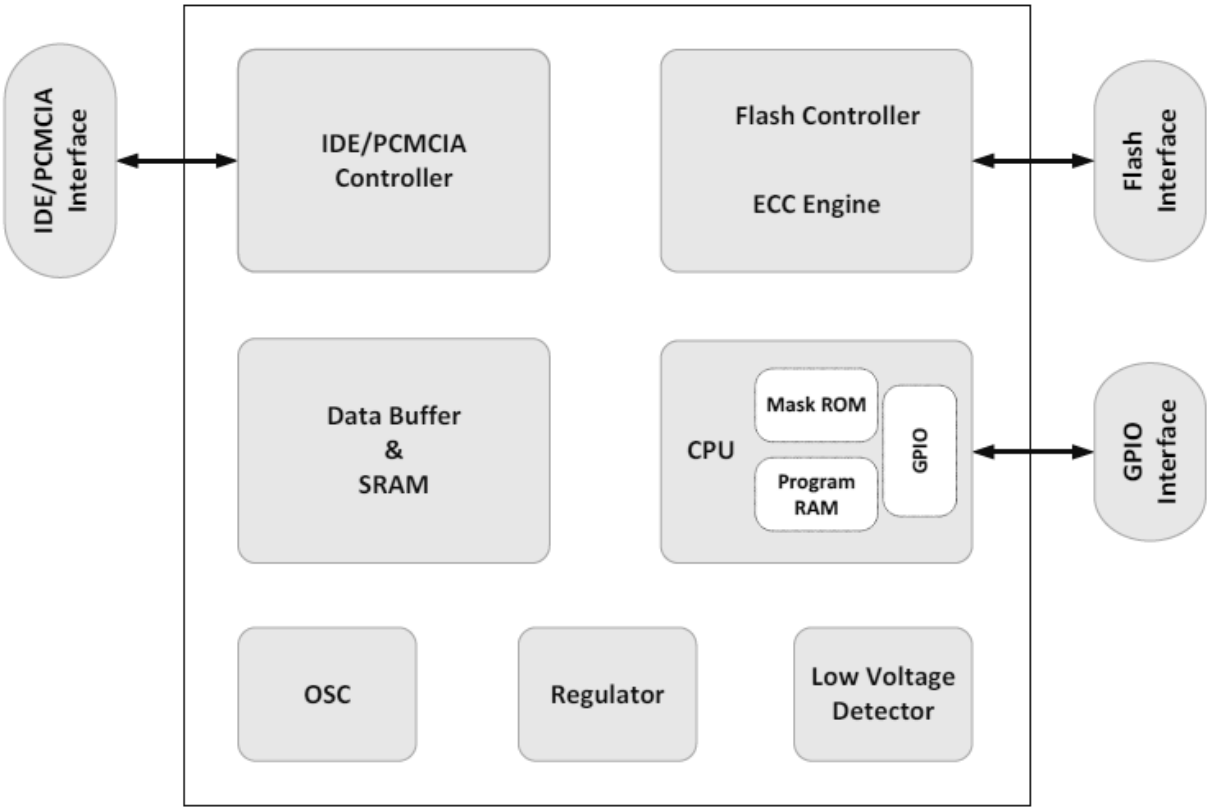


Figure 2-1: Functional block diagram

3. Pin Assignments

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CS0	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATA SEL	I
10	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOCS16	O	-IOCS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CS1	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD	I
35	-IOWR	I	IOWR	I	-IOWR	I
36	-WE	I	-WE	I	-WE	I
37	READY	O	-IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	RESET	I
42	-WAIT	O	-WAIT	O	IORDY	O
43	-INPACK	O	-INPACK	O	DMARQ	O
44	-REG	I	-REG	I	-DMACK	I
45	BVD2	O	-SPKR	O	-DASP	I/O
46	BVD1	O	-STSCHG	O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

Remarks: 1. WE should be connected to VCC in True IDE mode
2. CSEL is the input pin for master/slave selection used in True IDE mode.

4. Product Specifications

4.1 Capacity

Default capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1.

Table 4-1: Capacity specifications

Capacity	Total bytes	Cylinders	Heads	Sectors	Max LBA
512 MB	512,483,328	993	16	63	1,000,944
1 GB	1,024,966,656	1,986	16	63	2,001,888
2 GB	2,048,901,120	3,970	16	63	4,001,760
4 GB	4,110,188,544	7,964	16	63	8,027,712
8 GB	8,195,604,480	15,830	16	83	16,007,040
16 GB	16,391,340,032	16,383	16	63	32,014,336
32 GB	32,019,316,736	16,383	16	63	62,537,728
64 GB	64,030,244,864	16,383	16	63	125,059,072

Display of total bytes varies from operating systems.
Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies
Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Table 4-2: Performance specifications

Capacity / Performance	512 MB	1 GB	2 GB	4 GB	8 GB	16 GB	32 GB	64 GB
Sustained read (MB/s)	30	24	46	46	60	60	60	80
Sustained write (MB/s)	19	18	34	40	50	55	55	75

Notes: performance may vary depending on flash configurations or host system settings.

4.3 Environmental Specifications

Environmental specification of the Compact Flash Card series (CFC) follows the MIL-STD-810F.

Table 4-3: Environmental specifications

Environment		Specification
Temperature	Operation	0°C to 70°C; -40°C to 85°C (Extended Temperature)
	Storage	-40°C to 85°C
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operating)		20G
Shock (Non-Operating)		1,500G (0.5 msec)

4.4 Certification & Compliance

The CompactFlash card complies with the following global standards:

- CE
- FCC
- EMC
- RoHS

5. Software Interface

5.1 CF-ATA Command Set

Table 5-1 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 5-1: CFC-ATA command set

Command	Code
ERASE SECTOR(S)	C0h
EXECUTE DEVICE DIAGNOSTIC	90h
FORMAT TRACK	50h
FLUSH CACHE	E7h
IDENTIFY DEVICE	ECh
IDENTIFY DEVICE DMA	Eeh
INITIALIZE DRIVE PARAMETERS	91h
MEDIA LOCK	Deh
MEDIA UNLOCK	Deh
NOP	00h
READ BUFFER	E4h
READ DMA	C8h, C9h
READ LONG	22h, 23h
READ MULTIPLE	C4h
READ SECTOR(S)	20h, 21h
READ VERIFY SECTOR(S)	40h, 41h
RECALIBRATE	1Xh
REQUEST SENSE	03h
SEEK	7Xh
SET FEATURES	Efh
SET MULTIPLE MODE	C6h
TRANSLATE SECTOR	87h
WRITE BUFFER	E8h
WRITE DMA	Cah, CBh
WRITE LONG	32h, 33h
WRITE MULTIPLE	C5h
WRITE MULTIPLE without ERASE	CDh
WRITE SECTOR(S)	30h, 31h
WRITE SECTOR(S) without ERASE	38h
WRITE VERIFY	3Ch

6. Operating Conditions

Table 6-1: Operating range

Parameters	Range
Ambient temperature	0°C to 70°C
Extended temperature	-40°C to 85°C
Supply voltage at 3.3V	3.135 ~ 3.465 V
Supply voltage at 5V	4.75 ~ 5.25 V

Table 6-2: Power consumption (typical)

Capacity / Mode	512 MB	1 GB	2 GB	4 GB	8 GB	16 GB	32 GB	64 GB
Active (mA)	130	130	160	165	190	190	205	250
Stand By (mA)	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5

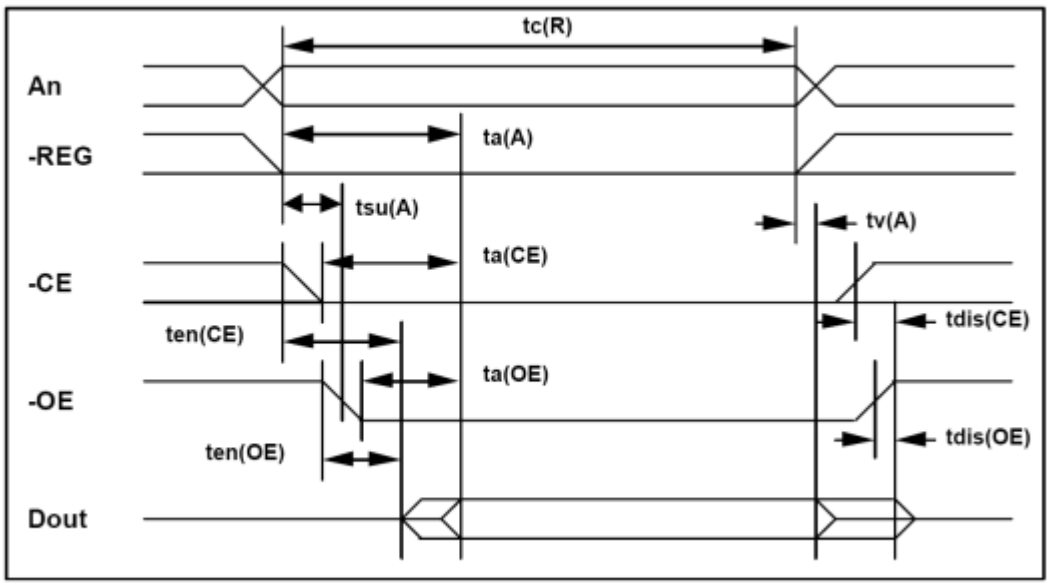
Note: Power consumptions were measured at 5V power supply and may vary depending on settings and platforms

7. AC Characteristics

7.1. PCMCIA Interface

7.1.1 Attribute Memory Read Timing

[Attribute Memory Read Timing]

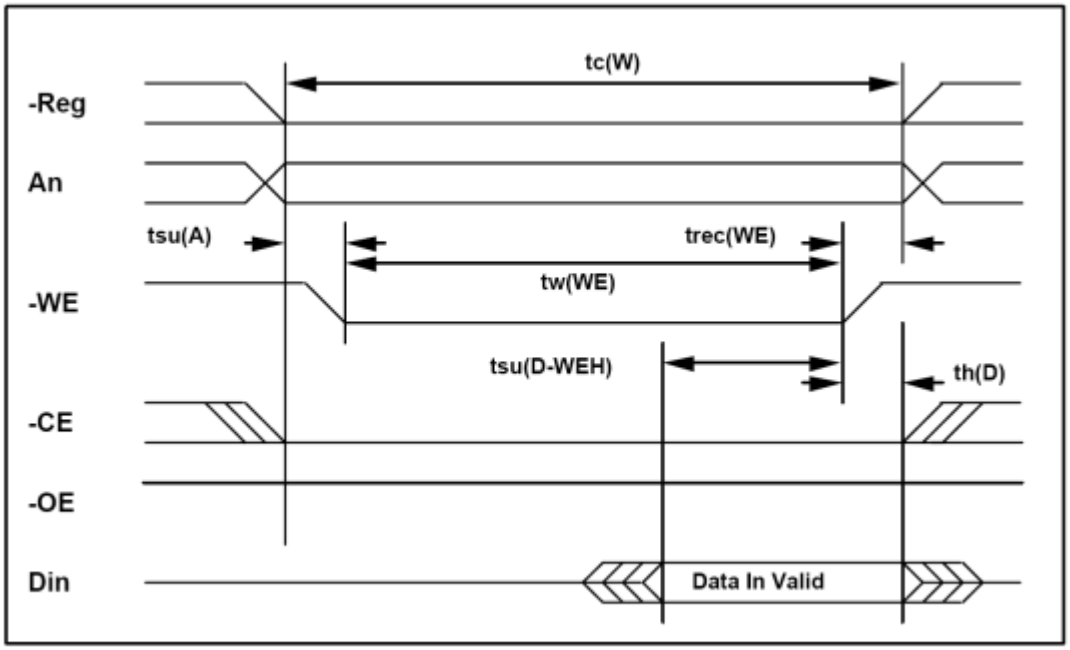


Attribute Memory Read Timing

Speed Version			100 ns		
Item	**Symbol**	**IEEE Symbol**	**Min[1]**	**Min[1]**	**Units**
Read Cycle Time	T_{CI}	tAVAV	300		ns
Address Access Time	$T_{A(A)}$	tAVQV		300	ns
Card Enable Access Time	$T_{A(CE)}$	tELQV		300	ns
Output Enable Access Time	$T_{A(OE)}$	tGLQV		150	ns
Output Disable Time from CE#	$T_{DIS(CE)}$	tEHQZ		100	ns
Output Disable Time from OE#	$T_{DIS(OE)}$	tGHQZ		100	ns
Address Setup Time	$T_{SU(A)}$	tAVGL	30		ns
Output Enable Time from CE#	$T_{EN(CE)}$	tELQNZ	5		ns
Output Enable Time from OE#	$T_{EN(OE)}$	tGLQNZ	5		ns
Data Valid from Address Change	$T_{V(A)}$	tAXQZ	0		ns

7.1.2 Attribute Memory Write Timing

[Attribute Memory Write Timing]

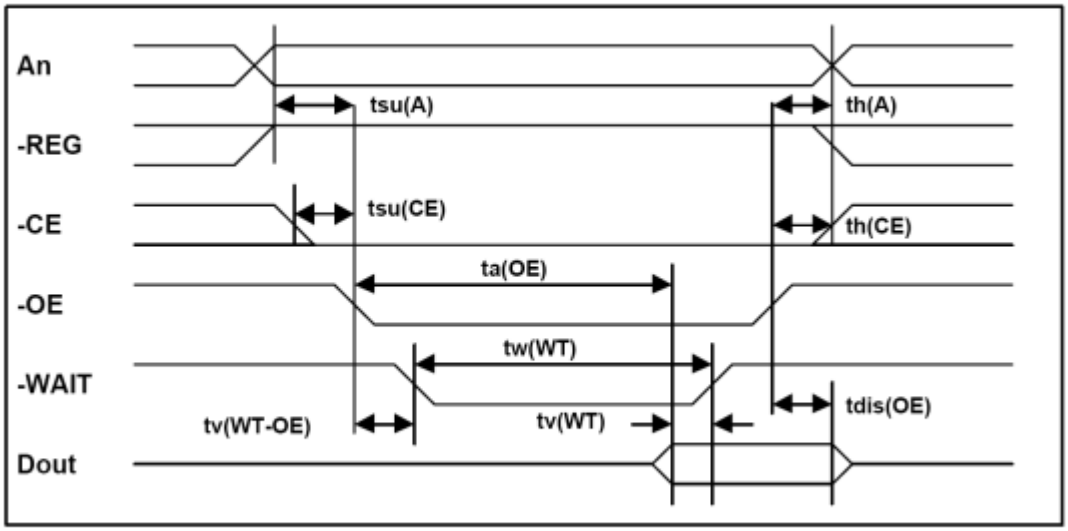


Attribute Memory Write Timing

Speed Version			250 ns		
Item	**Symbol**	**IEEE Symbol**	**Min[1]**	**Min[1]**	**Units**
Write Cycle Time	$T_{C(W)}$	tAVAV	250		ns
Write Pulse Width	$T_{W(WE)}$	tWLWH	150		ns
Address Setup Time	$T_{SU(A)}$	tAVWL	30		ns
Write Recover Time	$T_{REC(WE)}$	tWMAX	30		ns
Data Setup Time for WE	$T_{SU(DWE\#H)}$	tDVWH	80		ns
Data Hold Time	$T_{H(D)}$	tWMDX	30		ns

7.1.3 Common Memory Read Timing

[Common Memory Read Timing]



Common Memory Read Timing

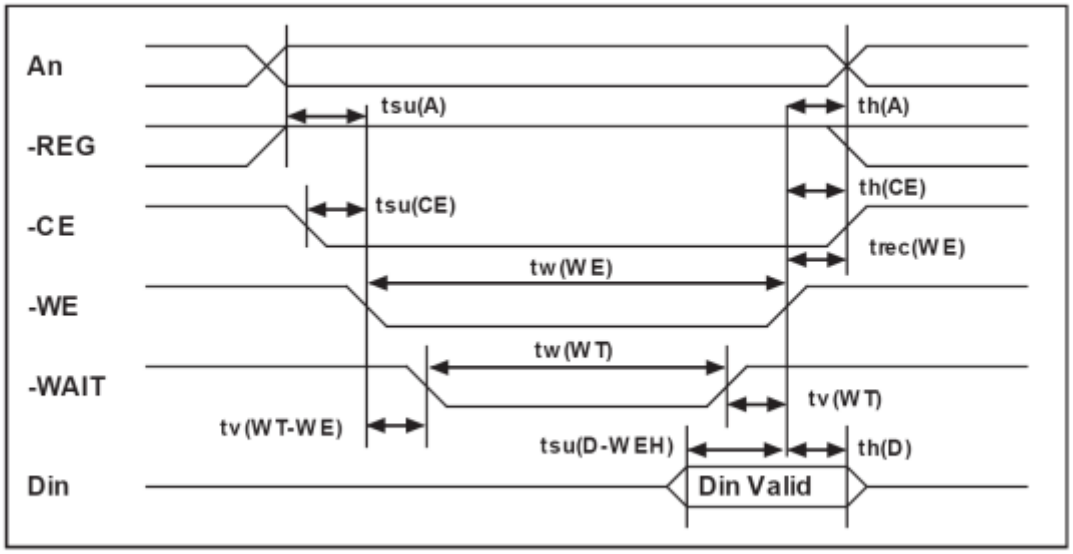
Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Output Enable Access Time	ta (OE)		125		60		50		45
Output Disable Time from HOE#	tdis (OE)		100		60		50		45
Address Setup Time	tsu (A)	30		15		10		10	
Address Hold Time	th (A)	20		15		15		10	
Cex# Setup before OE#	tsu (CE)	0		0		0		0	
Cex# Hold following OE#	th (CE)	20		15		15		10	
Wait Delay falling from OE#	tv (WT-OE)		35		35		35		Na
Data Setup for Wait Release	tv (WT)		0		0		0		Na
Wait Width Time	tw (WT)		350		350		350		Na

Note:

1. -WAIT is not supported in this mode.
2. The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load.
   All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

7.1.4 Common Memory Write Timing

[Common Memory Write Timing]



Common Memory Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before WE#	tsu (D-WEH)	80		50		40		30	
Data Hold following WE#	th (D)	30		15		10		10	
WE# Pulse Width	tw (WE)	150		70		60		55	
Address Setup Time	tsu (A)	30		15		10		10	
Cex# Setup before WE#	tsu (CE)	0		0		0		0	
Write Recovery Time	trec (WE)	30		15		15		15	
Address Hold Time	th (A)	20		15		15		15	
Cex# Hold following WE#	th (CE)	20		15		15		10	
Wait Delay falling from WE#	tv (WT-WE)		35		35				Na
WE# High from Wait Release	tv (WT)	0		0		0		Na	
Wait Width Time	tw (WT)		350		350		350		Na

Note:

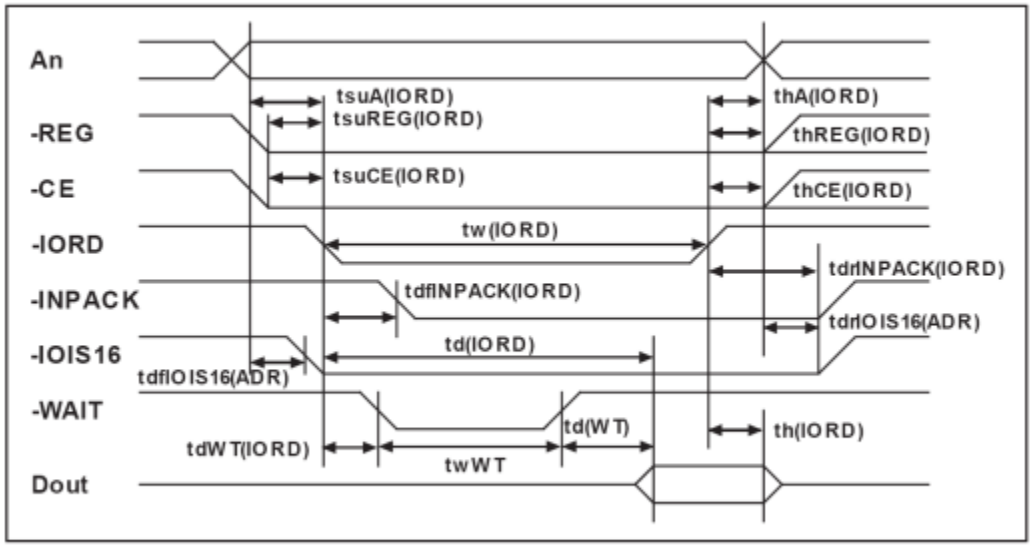
111.1 –WAIT is not supported in this mode.

111.2 The maximum load on –WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load.

All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The –WAIT signal may be ignored if the –WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

7.1.5 I/O Input Read Timing

[I/O Read Timing]



I/O Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Delay after IORD	td (IORD)		100		50		50		45
Data Hold following IORD	th (IORD)	0		5		5		5	
IORD Width Time	tw (IORD)	165		70		65		55	
Address Setup before IORD	tsuA (IORD)	70		25		25		15	
Address Hold following IORD	thA (IORD)	20		10		10		10	
CE Setup before IORD	tsuCE (IORD)	5		5		5		5	
CE Hold following IORD	thCE (IORD)	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	5		5		5		5	
REG Hold following IORD	thREG (IORD)	0		0		0		0	
INPACK Delay Falling from IORD	tdfNPACK (IORD)	0	45	0	na	0	na	0	na
INPACK Delay Rising from IORD	tdrNPACK (IORD)		45		na		na		na
IOIS16 Delay Falling from Address	tdfIOIS16 (ADR)		35		na		na		na
IOIS16 Delay Rising from Address	tdrIOIS16 (ADR)		35		na		na		na

Wait Delay falling from IORD	tdWT (IORD)		35		35		35		Na
Data Delay from Wait Rising	td (W T)		0		0		0		na
Wait Width Time	tw (W T)		350		350		350		Na

Notes:

1. -IOIS16 and -INPACK are not supported in this mode.
2. -WAIT is not supported in this mode.
3. Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA PC Card specification of 12µs but is intentionally less in this spec.

7.2.6 I/O Output Write Timing

[I/O Write Timing]

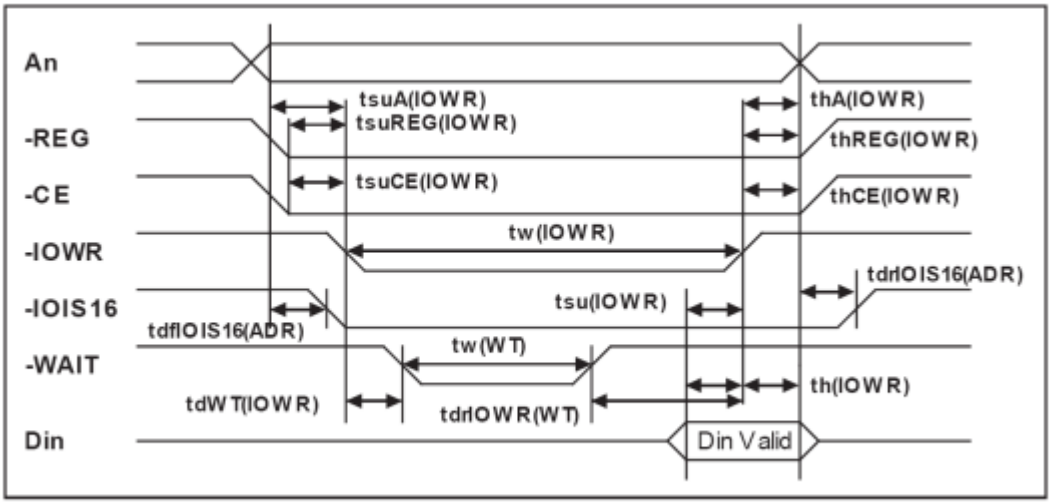


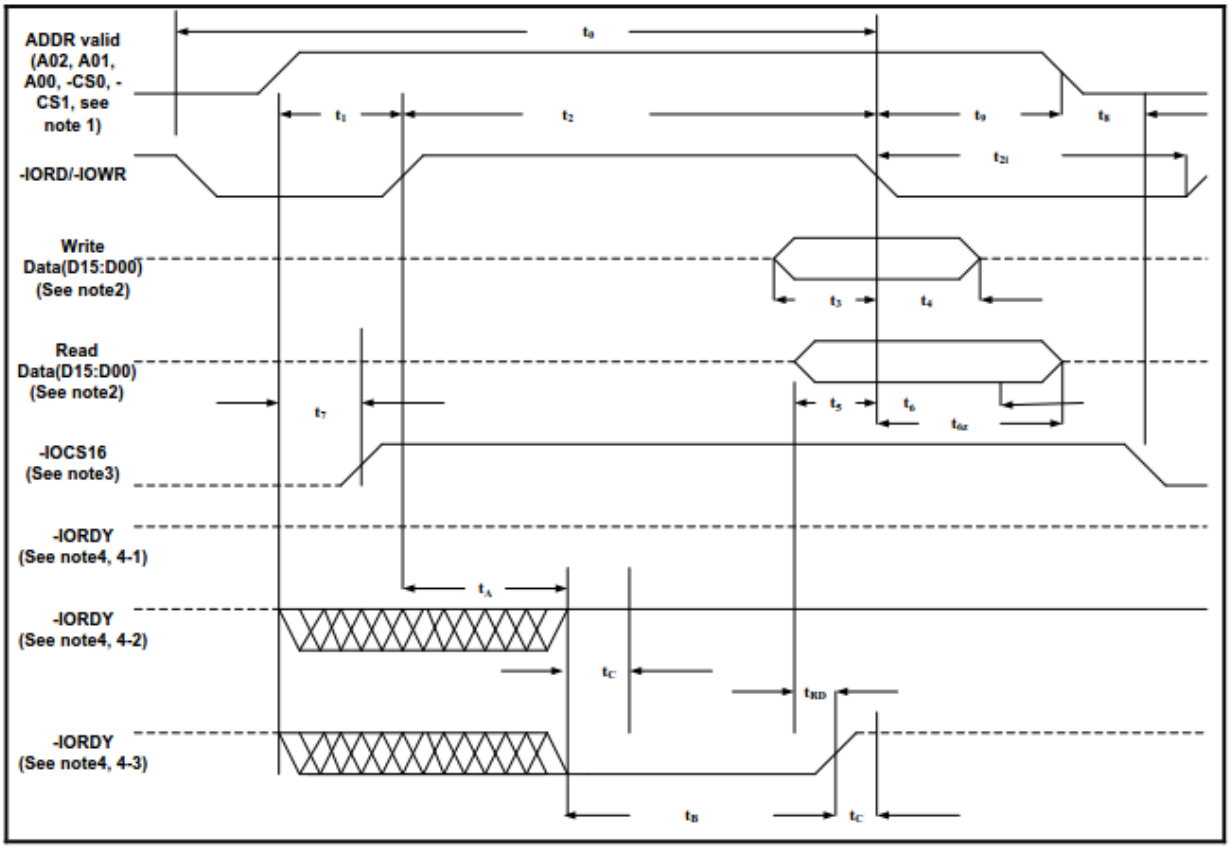
Figure 7: I/O Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
Data Setup before IOWR	tsu (IOWR)	60		20		20		15	
Data Hold following IOWR	th (IOWR)	30		10		5		5	
IOWR Width Time	tw (IOWR)	165		70		65		65	
Address Setup before IOWR	tsuA (IOWR)	70		25		25		15	
Address Hold following IOWR	thA (IOWR)	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	20		20		10		10	
REG Setup before IOWR	tsuREG (IOWR)	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16 (ADR)		35		na		na		na
IOIS16 Delay Rising from Address	tdrIOIS16 (ADR)		35		na		na		na
Wait Delay Falling from IOWR	tdWT (IOWR)		35		35		35		na
IOWR high from Wait High	tdrIOWR (WT)	0		0				0	
Wait Width Time	tw (W T)		350		350		350		na

Notes:

1. -IOIS16 and -INPACK are not supported in this mode.
2. -WAIT is not supported in this mode.
3. The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA PC Card specification of 12 µs but is intentionally less in this specification.

7.2 IDE Interface (PIO mode)



IDE Interface Timing (PIO Mode)

Notes:

1. Device address consists of -CS0, -CS1, and A[02:00]
2. Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
3. -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
   - 4.1. Device never negates IORDY: No wait is generated.
   - 4.2. Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
   - 4.3. Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

True IDE Mode Interface Timing

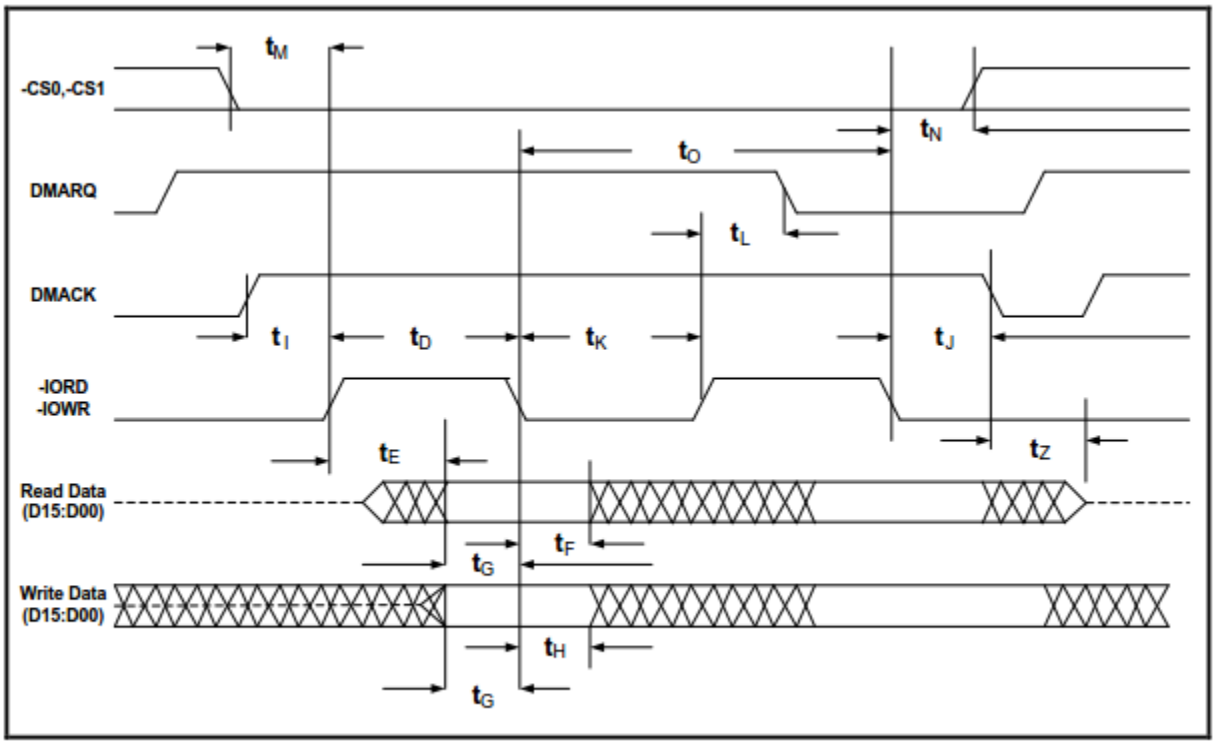
Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
Cycle Time (Min.)	t0	600	383	240	180	120	100	80
Address Valid to –IORD/-IOWR Setup (Min.)	t1	70	50	30	30	25	15	10
-IORD/-IOWR (Min.)	t2	165	125	100	80	70	65	55
-IORD/-IOWR (Min.) Register (8-bit)	t2	290	290	290	80	70	65	55
-IORD/-IOWR Recovery Time (Min.)	t2i	-	-	-	70	25	25	20
-IOWR Data Setup (Min.)	t3	60	45	30	30	20	20	15
-IOWR Data Hold (Min.)	t4	30	20	15	10	10	5	5
-IORD Data Setup (Min.)	t5	50	35	20	20	20	15	10
-IORD Data Hold (Min.)	t6	5	5	5	5	5	5	5
-IORD Data Tristate (Max.)	t6Z	30	30	30	30	30	20	20
Address Valid to IOCS16# Assertion (Max.)	t7	90	50	40	n/a	n/a	n/a	n/a
Address Valid to IOCS16# released (Max.)	t8	60	45	30	n/a	n/a	n/a	n/a
-IORD/-IOWR to Address Valid Hold	t9	20	15	10	10	10	10	10
Read Data Valid to IORDY Active (Min.), if IORDY initially low after tA	tRD	0	0	0	0	0	0	0
IORDY Setup Time	tA	35	35	35	35	35	Na	Na
IORDY Pulse Width (Max.)	tB	1250	1250	1250	1250	1250	Na	Na
IORDY Assertion to Release (Max.)	tC	5	5	5	5	5	Na	Na

Notes:

All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

1. t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).
3. The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.
4. t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.
5. IORDY is not supported in this mode.

7.3 Multi-Word DMA



Multi Word DMA

Notes:

1. If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
2. This signal may be negated by the host to suspend the DMA transfer in progress.

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

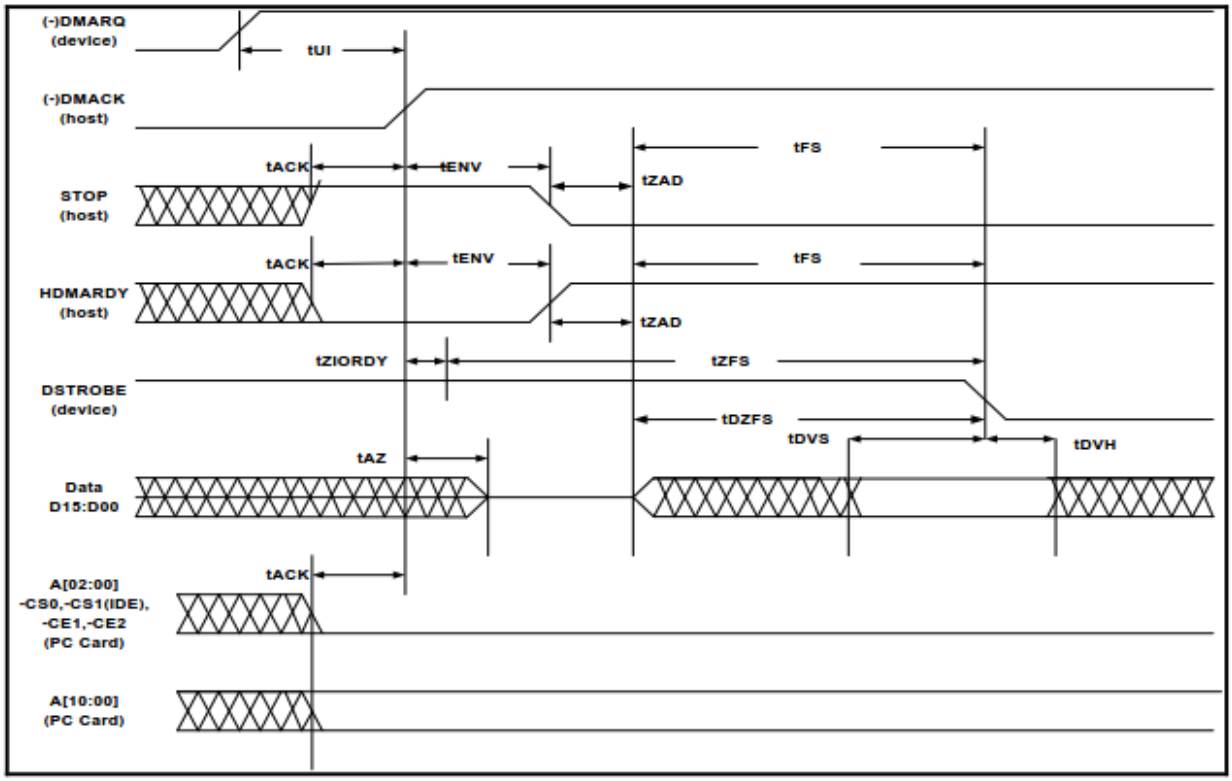
Multi-Word DMA

Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
Cycle Time (Min.)	tO	480	150	120	100	80
-IORD/-IOWR asserted width (Min.)	tD	215	80	70	65	65
-IORD data access (Max.)	tE	150	60	50	50	45
-IORD data hold (Min.)	tF	5	5	5	5	5
-IORD/-IOWR data setup (Min.)	tG	100	30	20	15	10
-IOWR data hold (Min.)	tH	20	15	10	5	5
DMACK to –IORD/-IOWR setup (Min.)	tI	0	0	0	0	0
-IORD/-IOWR to –DMACK hold (Min.)	tJ	20	5	5	5	5
-IORD negated width (Min.)	tKR	50	50	25	25	20
-IOWR negated width (Min.)	tKW	215	50	25	25	20
-IOWR to DMARQ delay (Max.)	tLR	120	40	35	35	35
-IOWR to DMARQ delay (Max.)	tLW	40	40	35	35	35
CS(1:0) valid to –IORD/-IOWR	tM	50	30	25	10	5
CS(1:0) hold	tN	15	10	10	10	10
-DMACK	tz	20	25	25	25	25

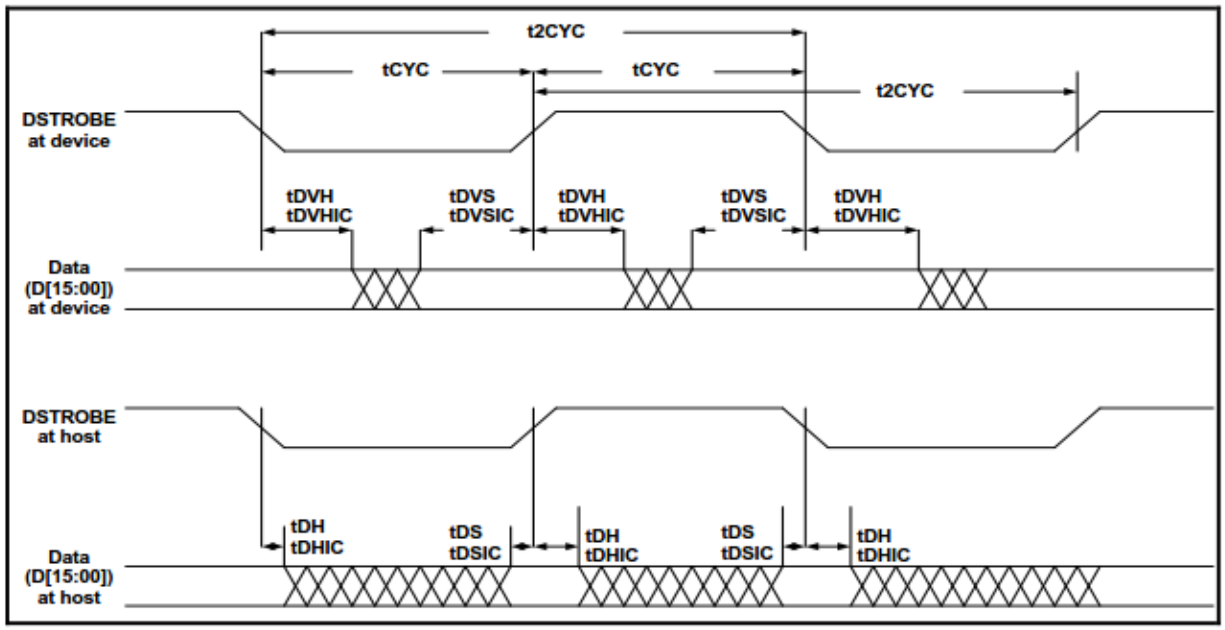
Note:

1. t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR} and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D, t_{KR} and t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} and t_{KW} as needed to ensure that t_D is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

7.4 Ultra DMA



To Initialize an Ultra DMA Data in Burst Timing



Sustained Ultra DMA Data-in Burst Timing

Ultra DMA Burst Timing

Parameter	UDMA Mode 0	UDMA Mode 1	UDMA Mode 2	UDMA Mode 3	UDMA Mode 4	UDMA Mode 5	Measure Location
$t_{2CYCTYP}$	240	160	120	90	60	40	Sender
t_{CYC}	112	73	54	39	25	16.8	See note
t_{2CYC}	230	153	115	86	57	38	Sender
t_{DS}	15.0	10.0	7.0	7.0	5.0	4.0	Recipient
t_{DH}	5.0	5.0	5.0	5.0	5.0	4.6	Recipient
t_{DVS}	70.0	48.0	31.0	20.0	6.7	4.8	Sender
t_{DVH}	6.2	6.2	6.2	6.2	6.2	4.8	Sender
t_{CS}	15.0	10.0	7.0	7.0	5.0	5.0	Device
t_{CH}	5.0	5.0	5.0	5.0	5.0	5.0	Device
t_{CVS}	70.0	48.0	31.0	20.0	6.7	10.0	Host
t_{CVH}	6.2	6.2	6.2	6.2	6.2	10.0	Host
t_{ZFS}	0	0	0	0	0	35	Device
t_{DZFS}	70.0	48.0	31.0	20.0	6.7	25	Sender
t_{FS}	230	200	170	130	120	90	Device
t_{LI}	0 – 150	0 – 150	0 – 150	0 – 100	0 – 100	0 – 75	See note
t_{MLI}	20	20	20	20	20	20	Host
t_{UI}	0	0	0	0	0	0	Host
t_{AZ}	10	10	10	10	10	10	See note
t_{ZAH}	20	20	20	20	20	20	Host
t_{ZAD}	0	0	0	0	0	0	Device
t_{ENV}	20 – 70	20 – 70	20 – 70	20 – 55	20 – 55	20 – 50	Host
t_{RFS}	75	70	60	60	60	50	Sender
t_{RP}	160	125	100	100	100	85	Recipient
t_{IORDYZ}	20	20	20	20	20	20	Device
t_{ZIORDY}	0	0	0	0	0	0	Device
t_{ACK}	20	20	20	20	20	20	Host
t_{SS}	50	50	50	50	50	50	Sender

Notes:
All timing are in nanoseconds and all timing measurement switching points (low to high and high to low) are taken at 1.5V. All signal transitions for a timing parameter are determined at the connector specified in the measurement location column. Parameter t_{CYC} is determined at the connector of the recipient farthest from the sender, while parameter t_{LI} is determined at the connector of a sender or recipient responding to an incoming transition from the recipient or sender, respectively. Both incoming signal and outgoing response are determined at the same connector. Parameter t_{AZ} is determined at the connector of a sender or recipient driving the bus, and must release the bus to allow for a bus turnaround.

Ultra DMA Burst Timing

Parameter	UDMA Mode 6	UDMA Mode 7
$t_{2CYCTYP}$	30	24
t_{CYC}	13	10
t_{2CYC}	29	23
t_{DS}	2.6	2.5
t_{DH}	3.5	2.9
t_{DVS}	4	2.9
t_{DVH}	4	3.2
t_{CS}	5	5
t_{CH}	5	5
t_{CVS}	10	10
t_{CVH}	10	10
t_{ZFS}	25	15
t_{DZFS}	17.5	10.5
t_{FS}	80	70
t_{LI}	0-60	0-50
t_{MLI}	20	20
t_{UI}	0	0
t_{AZ}	10	10
t_{ZAH}	20	20
t_{ZAD}	0	0
t_{ENV}	20-50	20-50
t_{RFS}	50	50
t_{RP}	85	85
t_{IORDYZ}	20	20
t_{ZIORDY}	0	0
t_{ACK}	20	20
t_{SS}	50	50

Ultra DMA Burst Timing Descriptions

Parameter	Description & Comment	Note
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
t_{DVS}	Data valid setup at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time at device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK(#) negation)	3
t_{CVH}	CRC word valid hold time at sender (from DMACK(#) negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing)	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drives to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	Drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from DMACK(#)) to STOP and HDMARDY# during data in burst initiation and from DMACK(#) to STOP during data out burst initiation	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY#)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY#)	
t_{IORDYZ}	Maximum time before releasing IORDY	6
t_{ZIORDY}	Minimum time before driving IORDY	4, 6
t_{ACK}	Setup and hold times for DMACK(#) (before assertion or negation	
t_{SS}	Time from STROBE edge to negation of DMARQ(#) or assertion of STOP (when sender terminates a burst)	

Notes:
1. Parameters tUI, tMLI and tLI represent sender-to-recipient or recipient-to-sender interlocks, for instance, one agent (sender or recipient) is waiting for the other agent to respond with a signal before proceeding. Parameter tUI denotes an unlimited interlock that

has no maximum time value; tMLI represents a limited time-out that has defined minimum; tLI is a limited time-out that has a defined maximum.
2. The 80-conductor cabling is required to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes exceeding 2.
3. Timing for tDVS, tDVH, tCVS, and tCVH must be met for lumped capacitive loads of 15 and 40 pF at the connector where the data and STROBE signals have the same capacitive load value.
4. Fall all timing modes, parameter tZIORDY may be greater than tENV since the host has a pull up on IORDY giving it a known state when released.
5. Parameters tDS and tDH for mode 5 are defined for a recipient at the end of a cable only in a configuration that has a single device located at the cable end. This configuration can result in tDS, and tDH for mode 5 at the middle connector having minimum values of 3.0 and 3.9 nanoseconds respectively.
6. The parameters are only applied to True IDE mode operation.

8. Mechanical Specifications

8.1 Dimensions

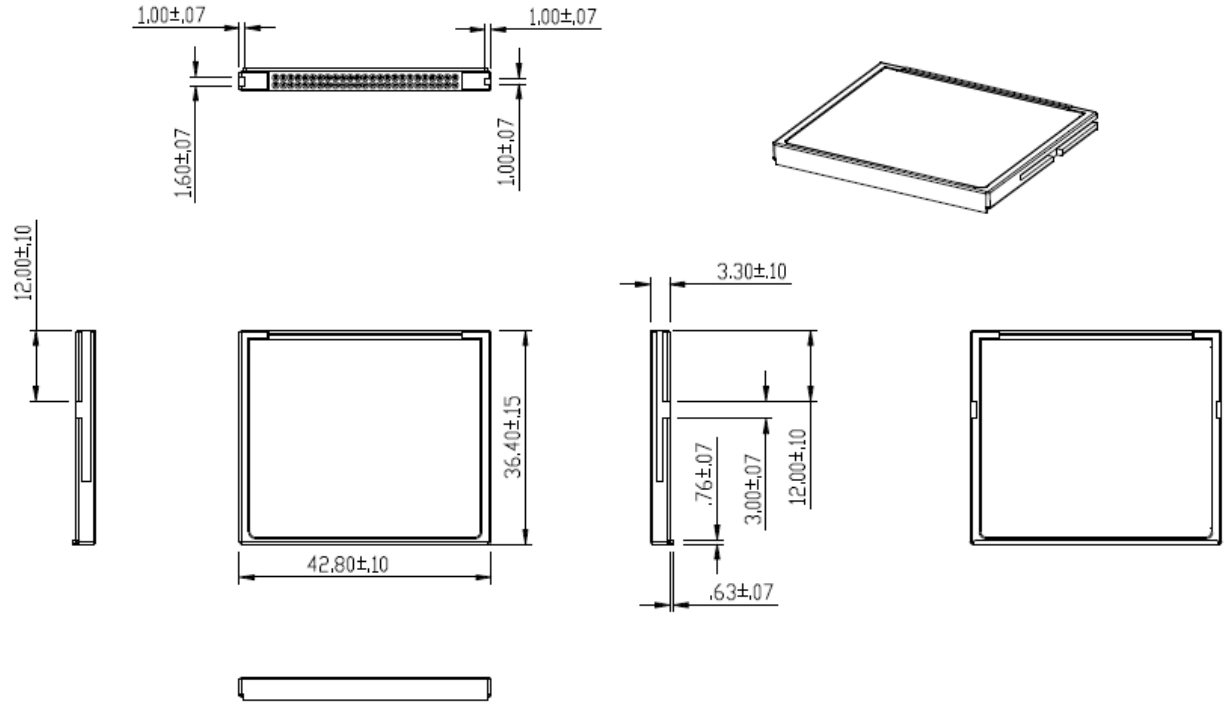


FIGURE 7-1: Physical dimension

Unit: mm

9. Product Ordering Information

9.1 Product Code Designations

AP – CF xxxx 4 A N S – XXXX X

FW

Specification
NR: Non-Removable
ET: Extended Temperature
ETNR: Ext. Temp. + Non-Removable

Halogen Free Compliant

Configuration

N=Standard

CTL Type

CFC Type

Capacities:

512M	512MB
001G	1GB
002G	2GB
004G	4GB
008G	8GB
016G	16GB
032G	32GB
064G	64GB

Model Name

Apacer Product Code

9.2 Valid Combinations

9.2.1 Standard Temperature

Non-Removable

Capacity	*AP/N*
512MB	AP-CF512M4ANS-NR
1GB	AP-CF001G4ANS-NR
2GB	AP-CF002G4ANS-NR
4GB	AP-CF004G4ANS-NR
8GB	AP-CF008G4ANS-NR
16GB	AP-CF016G4ANS-NR
32GB	AP-CF032G4ANS-NR
64GB	AP-CF064G4ANS-NR

9.2.2 Extended Temperature

Ext. Temp. + Non-Removable

Capacity	*AP/N*
512MB	AP-CF512M4ANS-ETNR
1GB	AP-CF001G4ANS-ETNR
2GB	AP-CF002G4ANS-ETNR
4GB	AP-CF004G4ANS-ETNR
8GB	AP-CF008G4ANS-ETNR
16GB	AP-CF016G4ANS-ETNR
32GB	AP-CF032G4ANS-ETNR
64GB	AP-CF064G4ANS-ETNR

Note: Please consult with Apacer sales representatives for availabilities.

Revision History

Revision	Date	Description	Remark
1.0	11/13/2014	Official Released	
1.1	03/16/2015	Added section 1.2.3 Error Correction/Detection	

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