Uncorrectable Bit Error Rate (UBER)

White Paper

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1. Overview

NAND flash memory exhibits a couple of inherent constraints. The two most characteristic are (1) limited lifespan because NAND flash memory deteriorates with use and eventually wears out, and (2) naturally appearing bit error rates because random bit errors can be generated in the stored data, due to that oxide layer for an FGMOS can degrade overtime and therefore will become unable to store charges properly on the floating gate. On top of that, as the manufacturing process of NAND flash has been continuously scaled to smaller nanometer, and the widespread adoption of flash technology in both consumer electronics and industrial applications has shifted from single-level cell (SLC) to multi-level cell (MLC) which can store two bits of information in the same physical space that SLC stores one bit, the number of program/erase cycles each cell can endure is decreased, thereby further reducing useful life for flash-based storage systems.

The raw bit error rate (RBER) in NAND flash memory increases proportionally with the number of P/E cycles. Stronger error correcting codes (ECC) can detect and correct more error rates, but these inevitably provides diminishing returns in number of P/E cycles [1]. The bit error rate occurs by nature indicates the four types of errors including read errors, program errors, erase errors, and retention errors that happen over the lifetime of a flash cell during read, program, and erase operations. These errors which represent corrupted data need to be resolved by ECC. However, some errors may still remain after error correction because the error correction capability of ECC is not strong enough. The errors that failed to be corrected are uncorrectable bit error rate (UBER).

In the following chapters, definitions of RBER and UBER and the relationship between UBER and NAND flash characteristics over flash lifetime will be elaborated in detail by referring to the reports and literature published by authoritative organizations in the NAND flash industry.

2. Term Explanations

NAND flash memory exhibits four types of naturally occurring errors that happen over the lifetime of a flash cell during read, program, and erase operations. These inherent errors include read, erase, and program errors caused by common flash operations, and retention errors caused by flash cell losing charge over time. Depending on the type of error appearing, following consequences can be observed:

- **Read errors**: The read disturb can lead to a significant increase in read errors.
- **Erase errors**: The protected or cacheable flash sector can lead to erase error.
- **Program errors**: The program disturb can lead to an increase in read errors.
- **Retention errors**: Data retention can lead to an increase in read errors with time.

According to the findings by Cai et al., the four types of errors are highly correlated with the number of P/E cycles each cell can tolerate. The maximum number of P/E cycles after which the ECC in an SSD can no longer guarantee the commonly required storage reliability (less than 10^{-15} UBER based on JEDEC standard as shown in Table 3-1) within a certain guaranteed data storage time is defined as the lifetime of flash block. Once P/E cycles of the SSD increase/exceed its guaranteed period, the raw bit error rate increases exponentially [2].

Table 3-1 SSD Classes and Requirements

Application Class	Workload (see JESD219)	Active Use (power on)	Retention Use (power off)	Functional Failure Requirement (FFR)	UBER Requirement
Client	Client	40°C 8 hrs/day	30°C 1 year	≤3%	$\leq 10^{-15}$
Enterprise	Enterprise	55°C 24 hrs/day	40°C 3 months	≤3%	$\leq 10^{-16}$

The errors must be resolved before the NAND flash becomes useable again. In order to detect and correct the errors, error correcting codes (ECC) are required. Depending on when ECC is applied, the errors representing the fraction of bits that contain incorrect data can be defined as raw bit error rate

(RBER) or uncorrectable bit error rate (UBER). Before applying ECC, the bit error rate is called RBER as suggested by the word “raw”; after applying ECC, it is called UBER which contains errors that cannot be corrected by ECC, as indicated by the word “uncorrectable”.

For more detailed definitions of and explanations about RBER and UBER, please see the following sections.

RBER (Raw Bit Error Rate)

The raw bit error rate (RBER), equivalent to bit error rate (BER), is the fraction of bits with erroneous data before error correction by ECC. Defined as the number of incorrect bits per number of total bits read including both correctable and uncorrectable bits, RBER can be considered a standard metric to evaluate flash reliability, which is evidenced by the statements presented in a paper named *A Large-Scale Study of Flash Memory Failures in the Field*, “[t]he bit error rate (BER) of an SSD is the rate at which errors occur relative to the amount of information that is transmitted from/to the SSD. BER can be used to gauge the reliability of data transmission across a medium” [3].

UBER (Uncorrectable Bit Error Rate)

For flash-based SSDs, UBER is an important reliability metric related to the SSD lifetime. As defined and standardized by the JEDEC Committee in 2010 by documents JESD218: Solid-State Drive (SSD) Requirements and Endurance Test Method , UBER is “a metric for data corruption rate equal to the number of data errors per bit read after applying any specified error-correction method” [4].

As mentioned in the previous section, RBER is the fraction of bits with erroneous data before error correction by ECC. However, even after applying ECC, data with uncorrectable errors might still exist because the capability of ECC to detect and correct errors in the raw data might not be strong enough. Hence, the fraction of bits with erroneous data after error correction is called uncorrectable bit error rate (UBER).

3. Conclusion

This white paper explains the definition of RBER, UBER and flash-based SSD reliability characteristics. The relationship between UBER and NAND flash characteristics over flash lifetime with respect to reliability can be illustrated by Micron's endurance test results as shown in Figure 1 and Figure 2.

Generally speaking, UBER is inversely proportional to ECC correctability regardless of the operating temperature at 85°C (See Figure 1) or 25°C (See Figure 2). With the operating temperature set at 85°C, SSDs with 3K P/E cycles have more data points corresponding to UBERs ranging from 1E-10 to 1E-04 and exhibit higher ECC correctability up to 60 bits, while SSDs with 300 P/E cycles have comparatively less data points and can only support up to approximately 29 bits. When the operating temperature is set at 25°C, the number of data points has dramatically decreased and can only detect and correct up to 23 bits and 13 bits for SSDs with 3K P/E cycles and 300 P/E cycles respectively. Based on the findings, we may come to the conclusions as follows:

- Higher temperatures lead to higher failure rates. NAND flash memory devices deployed in high temperature environments require higher ECC correctability to correct errors.
- Higher number of bits of ECC correctability can detect and correct more error occurrences. The higher the ECC correctability, the more the errors can be corrected. SSDs with high UBERs are expected to have more error rates and encounter more errors that may potentially go undetected and corrupt data than SSDs with low UBERs.

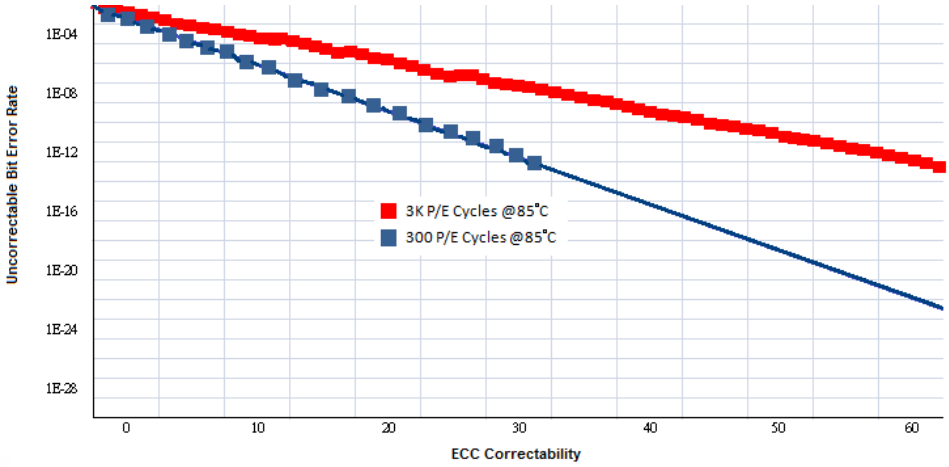

Figure 1 Endurance — 85°C UBER Data

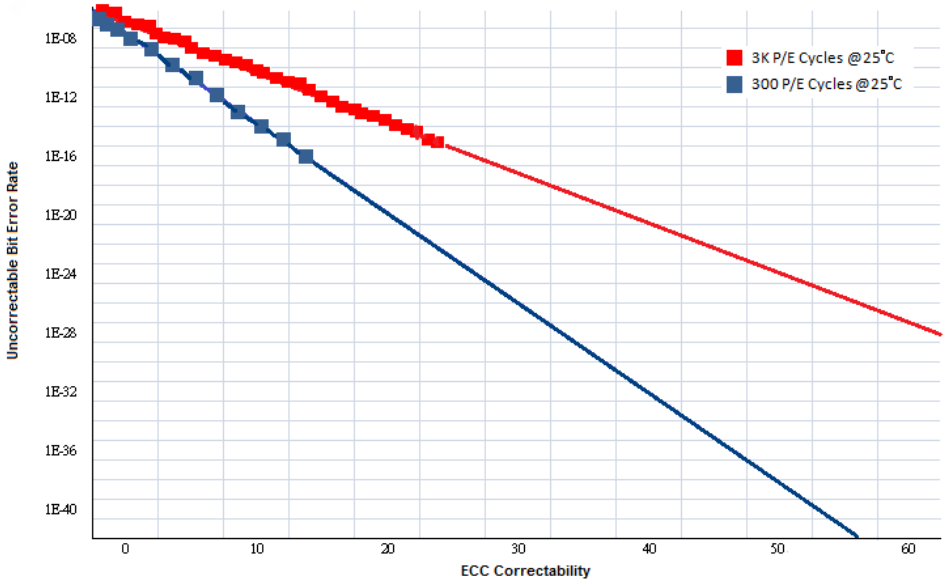

Figure 2 Endurance — 25°C UBER Data

References

[1] Y. Cai et al, “Flash Correct-and-Refresh: Retention-Aware Error Management for Increased Flash Memory Lifetime”, LSI Corporation, p.1

[2] Y. Cai et al, “Flash Correct-and-Refresh: Retention-Aware Error Management for Increased Flash Memory Lifetime”, LSI Corporation, p.2

[3] J. Meza, Q. Wu, S. Kumar, and O. Mutlu, “A Large-Scale Study of Flash Memory Failures in the Field”, p.3

[4] uncorrectable bit-error rate (UBER) JEDEC dictionary, JEDEC Committee (http://www.jedec.org/standards-documents/dictionary/terms/uncorrectable-bit-error-rate-uber)

Revision History

Revision	Date	Description	Remark
1.0	9/19/2016	Official release	

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