Apacer

NAND Flash Optimization Technologies

SLC-lite, SLC-liteX and MLC-liteX White Paper

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1. Introduction

NAND Flash has become a mature technology over the last few years. And the variety of formats that are now available are already adopted in many industrial applications. However, with the desire to go beyond the standard options, Apacer has developed certain optimizations of NAND Flash technology. The goal of these optimizations is to provide customers with the amount of P/E cycles that best suits their application. This white paper will discuss some recent developments in this field.

The following table shows the various names of Apacer Flash optimizations and the amount of P/E cycles each one offers.

Name	SLC-liteX	SLC	SLC-lite	MLC-liteX	3D TLC and 2D MLC
P/E Cycles	100,000*	60,000	20,000	10,000	3,000

Comparison of Apacer's NAND Flash Optimizations

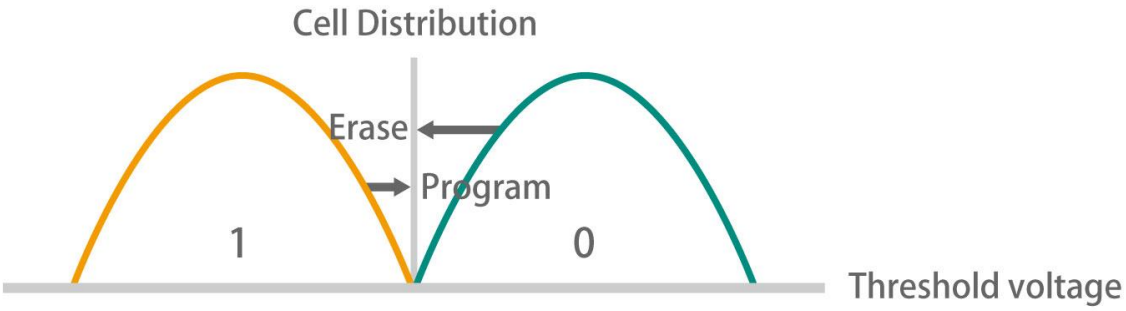
*Note: 100K P/E cycles are implemented on SATA and PCIe devices only, while USB devices and SD cards still remain at 30K P/E due to controller limitations.

2. How It Works

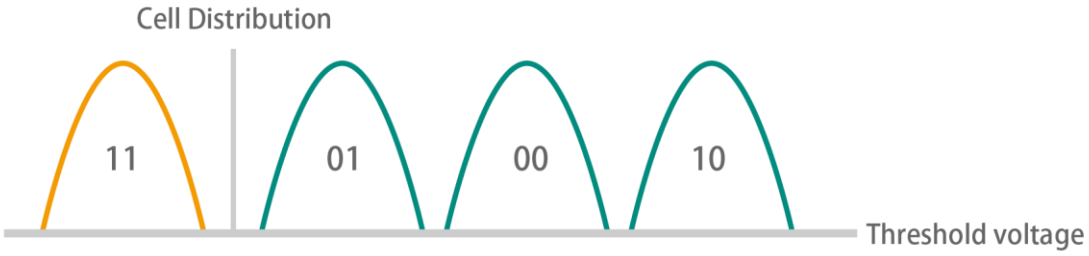
2.1 SLC vs. MLC

The basic idea behind SLC-lite technology is mainly the management of cell distribution. In a SLC NAND flash, only one bit is stored in each cell and therefore there are only two flash states “0” or “1” (0 for Programmed or 1 for Erase). The simple cell management of SLC makes it ideal for mission critical embedded or industrial applications.

SLC Cell Management



MLC Cell Management



SLC & MLC Cell Status

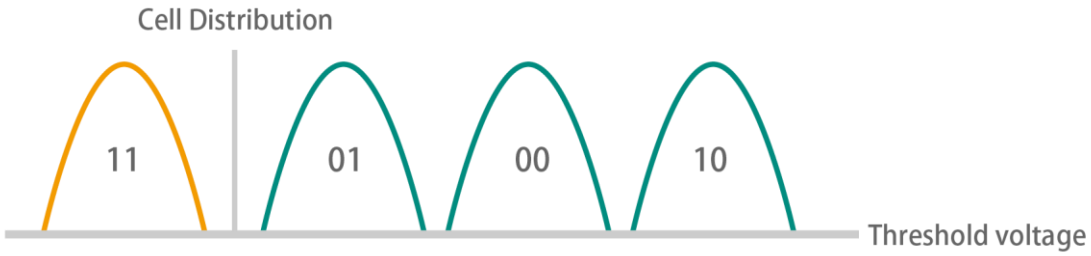
SLC	MLC	
0 (programmed)	11	10
1 (erased)	01	00

Since MLC can store two bits per cell, doubling the storing amount of SLC, MLC offers higher density and lower cost per bit. However, with more cells in the flash, it results in higher power consumption, lower endurance due to higher voltage delta required and the need of more precise charge placement and rigid controls of programming to ensure proper data flow. Therefore, SLC based storage media is often employed in industrial and embedded applications whereas MLC is often seen in consumer electronics.

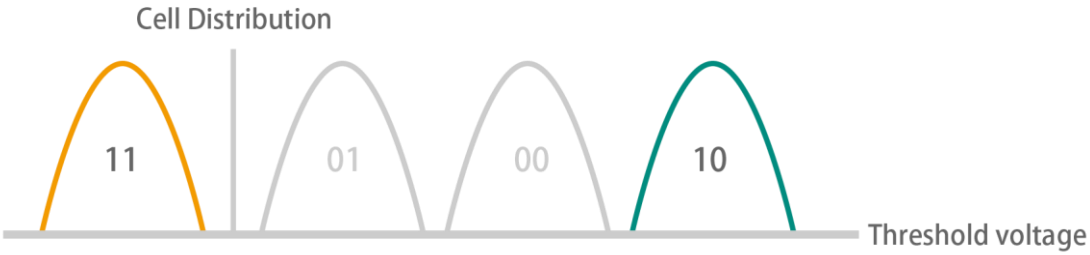
2.2 SLC-lite: The Balanced Solution

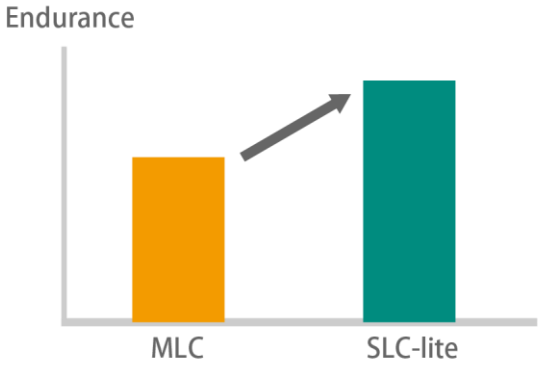
The central concept behind Apacer SLC-Lite is to make MLC behave like SLC. To achieve SLC-like performance and endurance, cell distribution management for MLC is necessary in order to greatly adjust the voltage delta and charge sensing. By programming only the least significant bit (LSB), the cell distribution behaves almost identical to that of SLC flash. This highly improves the precision of delta and the threshold voltage of each cell. Thus, the MLC performance and endurance, especially in P/E cycles, will be escalating by multiplies, to the level almost on par with SLC. In this case, users would get all the benefits of both the quality and the cost.

- How MLC works: programming both LSB (least significant bit) and MSB (most significant bit)

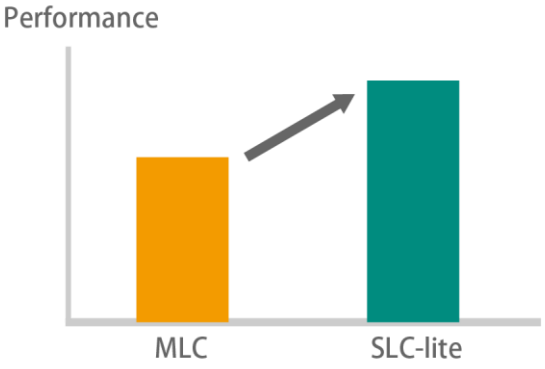


- By only programming the LSB, MLC will behave similarly to SLC. **This is SLC-lite.**





Greater endurance than MLC



Greater performance than MLC

More cost-effective than SLC

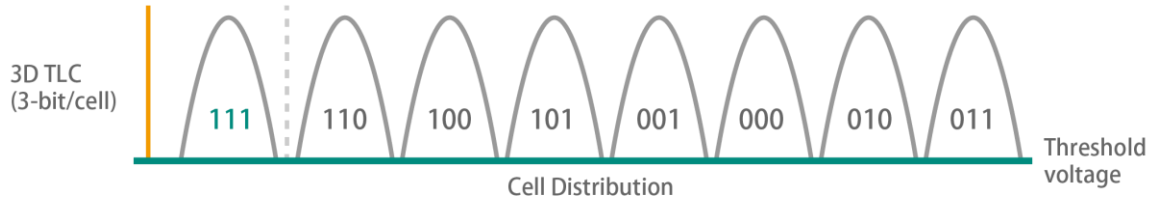
2.3 SLC-liteX and MLC-liteX

The central concept behind Apacer's SLC-lite is to make MLC behave like SLC. However, with the maturity of 3D NAND Flash technology, Apacer's engineers developed a similar process to SLC-lite for 3D NAND drives. The two new forms of this technology are called SLC-liteX and MLC-liteX.

SLC-liteX is based on 3D NAND technology. Apacer's engineers tweak the firmware to program less bits and increase program/erase cycles. They carefully select the NAND components, optimize the firmware and also employ specialized error handling algorithms. Together, these adjustments allow SLC-liteX to offer the greatest number of P/E cycles currently on the market – 100,000, which is 33 times more than MLC or industrial 3D TLC. The longest lifespans are therefore available at reasonable cost.

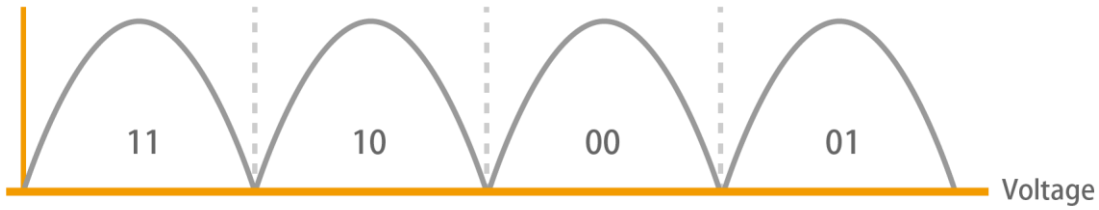
MLC-liteX is also based on 3D NAND technology. The firmware is fine-tuned in such a way as to offer more than three times as many P/E cycles (10,000) than MLC or industrial 3D TLC. Cost-benefit optimization is achieved while lifespans are still extended.

The standard bit format for 3D NAND TLC stores three bits in one cell. The following chart illustrates this format.



MLC-liteX programs only two of the three bits. So the capacity of MLC-liteX is only reduced by a third. The advantage of this tradeoff is that P/E cycles are increased. The following chart illustrates this programming architecture.

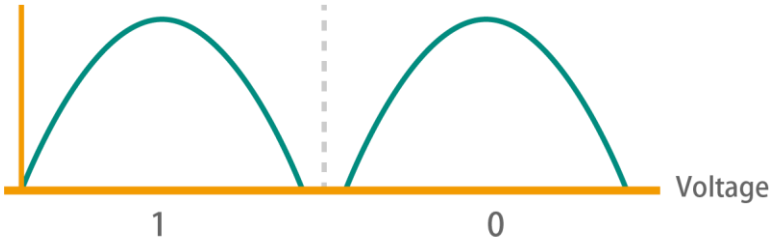
Read/Write Operation



Continuing in this vein, SLC-liteX programs only one of the three bits. The capacity is therefore reduced by two-thirds, but even more P/E cycles are available. The following chart illustrates this programming architecture.

Write Operation (one third of capacity)

Read Operation (better endurance)



The following table compares the three versions of 3D TLC directly.

	3D TLC	3D MLC-liteX	3D SLC-liteX
Bits per cell	3	2	1
P/E Count	3,000	10,000	100,000*
Performance	Good	Better	Excellent
Reliability	Good	Better	Excellent
Cost	$	$$	$$$
Capacity	★★★	★★	★

*Note: 100K P/E cycles are implemented on SATA and PCIe devices only, while USB devices and SD cards still remain at 30K P/E due to controller limitations.

3. Conclusion

The real benefit of these optimizations is flexibility. Depending on their needs, buyers can select the number of P/E cycles that they require. The tradeoff of capacity for endurance has proved an advantageous one for many customers. 3D NAND Flash optimization allows Apacer to deliver better value for money, and for our customers to produce devices that will function smoothly until they reach the end of their operational lifetimes.

Revision History

Revision	Description	Date
1.0	Official release	6/21/2019
1.1	Updated maximum number of SLC-liteX's P/E cycles.	9/30/2022

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