Apacer

Data Retention

White Paper

February 25, 2020

Version 1.5

Apacer Technology Inc.
1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

Table of Contents

1. Introduction

NAND flash-based storage has been the primary choice for industrial embedded systems. With no moving parts and a high number of input/output operations per second (IOPS), NAND flash-based devices are very effective in industrial applications and server systems. Although NAND flash-based storage provides higher performance than conventional storage, system designers may have some concerns about data reliability of using NAND flash-based storage and data retention is one of them.

Data retention is the measure of how long a flash cell would maintain its programmed state when the device is at an unpowered state. There are several factors which have impacts on data retention, including flash type, P/E cycles, usage patterns, temperature and etc. This white paper will provide a basic concept about data retention in flash-based storage. It will also explore the differences between SLC, MLC, 2D TLC and 3D TLC memory configurations, including advantages and disadvantages.

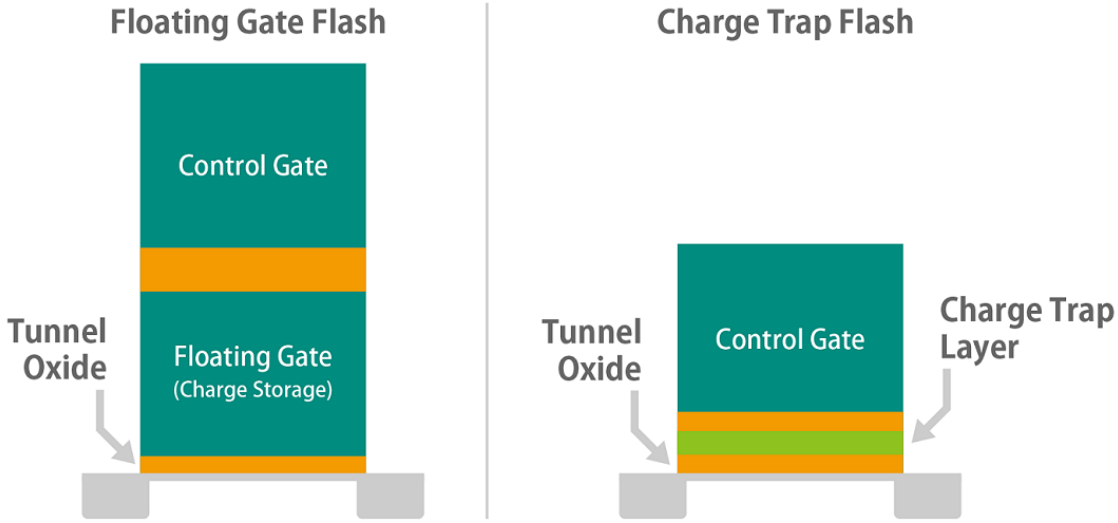
2. Flash Memory Basics

A NAND flash cell is basically a floating gate transistor. An extra gate, known as the floating gate, is added in between the control gate and the substrate. The floating gate is electronically isolated by an insulating oxide layer and has no electrical contacts. Charges within the floating gate will stay there for a long period of time. For flash memory devices, all the data is stored as charges on the floating gate.

Electrons flow between the control gate and the substrate. When a voltage is applied to the control gate, electrons are attracted upwards and tunnel through the thin oxide layer. The floating gate traps the electrons and an electric charge accumulates. This is the process to program the NAND cell. To erase a NAND cell, voltage is applied to the substrate forcing the electrons back through the oxide layer from the floating gate into the substrate and the charge is released from the floating gate.

The number of electrons at the floating gate causes a difference in the gate voltage. The voltage determines the bit signal which represents the data value. The data is read by checking the level of voltage on the cell. The insulating oxide layer wears out with the repeated tunneling of electrons. Over time, some electrons might be trapped at the floating gate or leaked back into the substrate, resulting in data loss.

Floating gate technology is standard for SLC and MLC memory types. However, some forms of 3D TLC memory are starting to adopt a new technology known as charge trap instead. Essentially, the advantage of charge trap technology is that the electrons in a floating gate are more free to move around, meaning they may eventually drift out of position, while electrons in a charge trap are barely able to move. Since 3D TLC memory is constructed vertically, charge trap technology is preferable because it’s easier to stack. However, manufacturers are still experimenting with upgrading both of these technologies at this time.

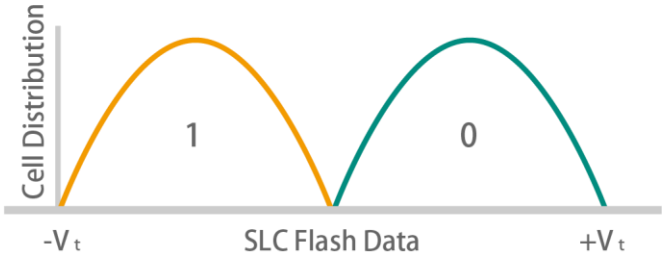


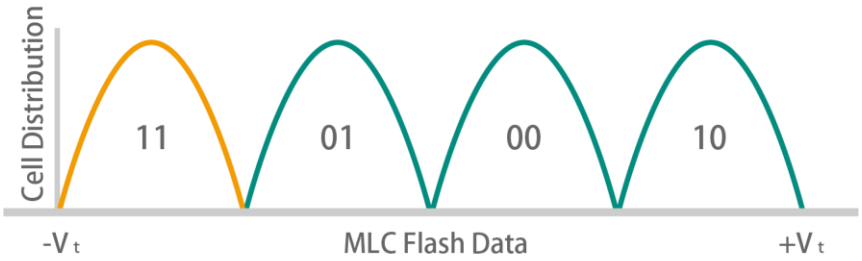
3. Flash Type & P/E Cycles

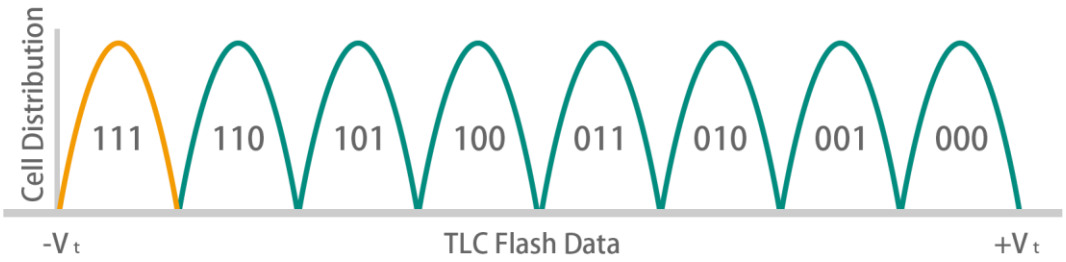
There are different flash technologies and trade-offs for each type. Single-level cell (SLC) uses a single cell to store one bit of data. Multi-level cell (MLC) memory is more complex and can interpret four digital states with two bits stored in a single cell. This makes production more cost effective but wears out faster. Triple-level cell (TLC) memory continues the trend in this direction, storing three bits in a single cell.

A side effect of storing more bits per cell is an increase in the rate of degradation of the flash cell. As mentioned in the previous chapter, the state of a NAND cell is determined by gate voltage, and the voltage is affected by the number of electrons present on the floating gate. For SLC, there are only two states to distinguish within the threshold voltage. For MLC, there are four states. A similar threshold voltage range will be divided into four regions. Therefore, MLC has less charge deviation before data errors occur. Continuing in this vein, TLC has eight states, meaning that degradation can become even more likely.

In addition to SLC, MLC and TLC, there’s also a technology known as SLC-lite. It uses a new NAND management system to store 1 bit on an MLC cell, giving it a performance and endurance ration somewhere between SLC and MLC. It’s ideal for situations where a balance between the advantages and disadvantages of these two memory types is preferable.







4. Usage Patterns

In general, flash memory does not degrade because of age, but rather because of the usage patterns which vary according to applications. The frequency of data being written and erased is expressed in program/erase (P/E) cycles. Memory that has endured a high number of P/E cycles has an increased rated of data degradation.

Different types of NAND flash cells have different wear endurance as well. The maximum number of times a flash cell can be programmed and erased is known as the P/E cycles. When NAND flash cells reach its maximum P/E cycles, they may flip enough bits to cause a high number of error bits. Bit flip occurs when a bit is switched from 0 to 1 or 1 to 0. When the error-correcting code (ECC) is unable to compensate, data loss will occur.

Type	SLC	SLC-lite	MLC	2D TLC	3D TLC	SLC-liteX
P/E Cycles	60,000	20,000	3,000	300 to 500	1,000-3,000	30,000
Note: only certain industrial-grade 3D TLC SSDs can reach 3,000 P/E cycles.						

Since the oxide layer degrades as the number of P/E cycles increases, the data retention decreases over time. After the initial stage, the estimated data retention follows an exponential decrease. Frequent P/E cycles will cause constant wear on the oxide layer of the flash cell. With a lower frequency of P/E cycles, the oxide layer will not be subjected to constant wear and will be able to recover and have a longer lifetime.

As the chart above also demonstrates, 2D TLC technology reduces the total amount of P/E cycles that are available to quite a low level – perhaps too low for some applications. But 3D TLC technology delivers just as many P/E cycles as MLC does, thanks to innovations in cell architecture. It does so while still remaining affordable and also offering superior data storage space.

5. Temperature

Temperature is another factor that has a great impact on data retention as the ability of NAND flash to retain data depends on the temperature which the flash cell is subjected to during active use and storage. With increased temperature the electrons escape the floating gate faster and the cell then changes the voltage state eventually. At high temperature, programming and erasing a flash cell is relatively less stressful to its structure as electrons leak at a faster rate, but data retention of a NAND cell suffers. At low temperature, data retention of the flash cell is enhanced. Electrons will also be stored easily but there is more stress to the cell structure, causing more wear to the oxide layer. Therefore, programming at a higher temperature and storage at a lower temperature will minimize the wear of the oxide layer.

The following data was based on tests and computer simulations. Data retention at a temperature of 40°C was evaluated. The first line shows typical P/E cycles near the beginning of a device's storage life, and the second line shows the same towards the end.

P/E Cycles	SLC Data Retention
6,000	10Y
60,000	1Y

P/E Cycles	SLC-lite Data Retention*
100	10Y
20,000	1Y

P/E Cycles	MLC Data Retention
300	10Y
3,000	1Y

P/E Cycles	SLC-liteX Data Retention**
100	10Y
30,000	1Y

P/E Cycles	3D TLC Data Retention
100	10Y
3,000	1Y

Note:

* This is estimated data retention based on computer simulations.

** The result of SLC-liteX is followed by JEDEC 219 client workload and tested at Apacer lab.

6. Conclusion

This paper has offered a fundamental overview of data retention. Users need to understand that there are several factors that affect data retention, especially usage patterns and environmental temperatures, which can vary significantly in industrial embedded applications. And users should also keep in mind that differences between SLC, MLC, 2D TLC and 3D TLC technology may also affect data retention. The greatest advantage of 3D TLC is that it supports comparable P/E cycles to MLC technology, while still offering greatly increased data storage at a competitive price.

Revision History

Revision	Description	Date
0.1	Preliminary release	11/30/2015
1.0	Official release	12/24/2015
1.1	- Revamped the layout - Made a couple of touch-ups on the content	9/21/2016
1.2	Updated the template	8/13/2018
1.3	Added information about 2D and 3D TLC, updated some diagrams	11/30/2018
1.4	Added SLC data retention table to 5. Temperature	2/17/2020
1.5	- Added SLC-liteX data retention table to 5. Temperature - Added SLC-liteX P/E cycles to 4. Usage Patterns	2/25/2020

Global Presence

Taiwan (Headquarters)
Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: 886-2-2267-8000
Fax: 886-2-2267-2261
amtsales@apacer.com

U.S.A.
Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9551
sa@apacerus.com

Japan
Apacer Technology Corp.
6F, Daiyontamachi Bldg., 2-17-12, Shibaura, Minato-Ku,
Tokyo, 108-0023, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe
Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China
Apacer Electronic (Shanghai) Co., Ltd
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD, Shanghai, 200051, China
Tel: 86-21-6228-9939
Fax: 86-21-6228-9936
sales@apacer.com.cn

India
Apacer Technologies Pvt Ltd,
1874, South End C Cross, 9th Block Jayanagar,
Bangalore-560069, India
Tel: 91-80-4152-9061/62
Fax: 91-80-4170-0215
sales_india@apacer.com